

ZZZ1

PCB
DAZ@

PJP1

45@DCIN

ZZZ2

LA-5981P
DA2@

ZZZ3

LS-5981P
DA2@

ZZZ4

LS-5982P
DA2@

ZZZ5

LS-5983P
DA2@

ZZZ6

LS-5984P
DA2@

ZZZ7

LS-5986P
DA2@

Compal Confidential

NCQF0 M/B Schematics Document

Intel Arrandale/Clarkfield Processor with DDRIII + Ibex Peak-M

2010-04-18

REV : 1 . A

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				Size	Document Number
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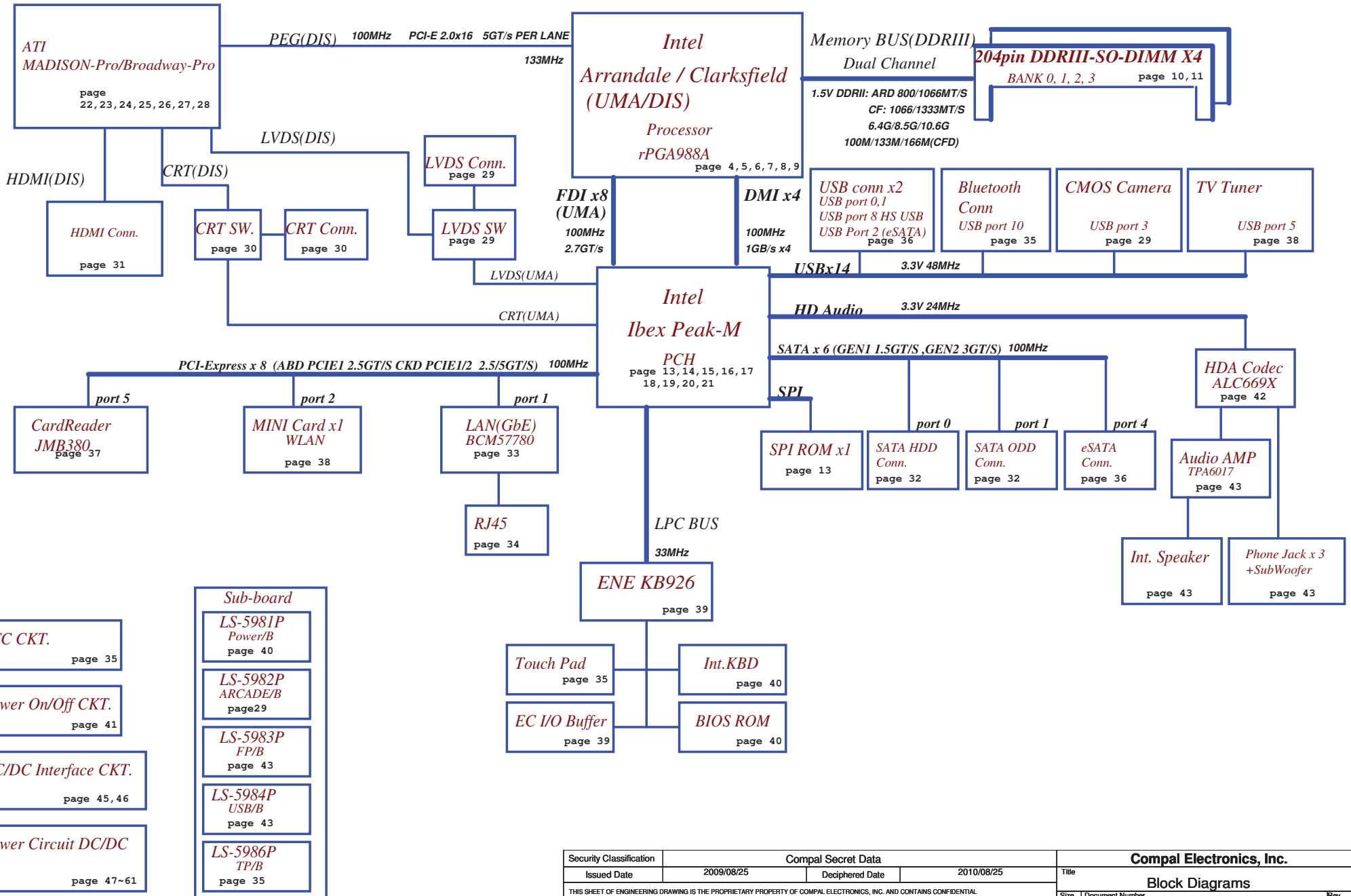
Compal Confidential

Model Name : NCQF0

File Name : LA5981P

Fan Control
page 44

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
27MHz no SSC to VGA
page 12



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								Size B	Document Number		NCQF0 M/B LA-5981P Schematic		Rev 1.0
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Power Plane	Description	S1	S3	S5	DGPU (UMA)	DGPU (DIS)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	ON	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF		
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3V	3.3V power rail for PCH	ON	ON	ON		
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+5V	5V power rail for PCH	ON	ON	ON		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+5VSDGPU	5V power rail for GPU				OFF	ON
+1.5VSDGPU	1.5V power rail for VRAM				OFF	ON
+1.8VSDGPU	1.8V switched power rail for GPU				OFF	ON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

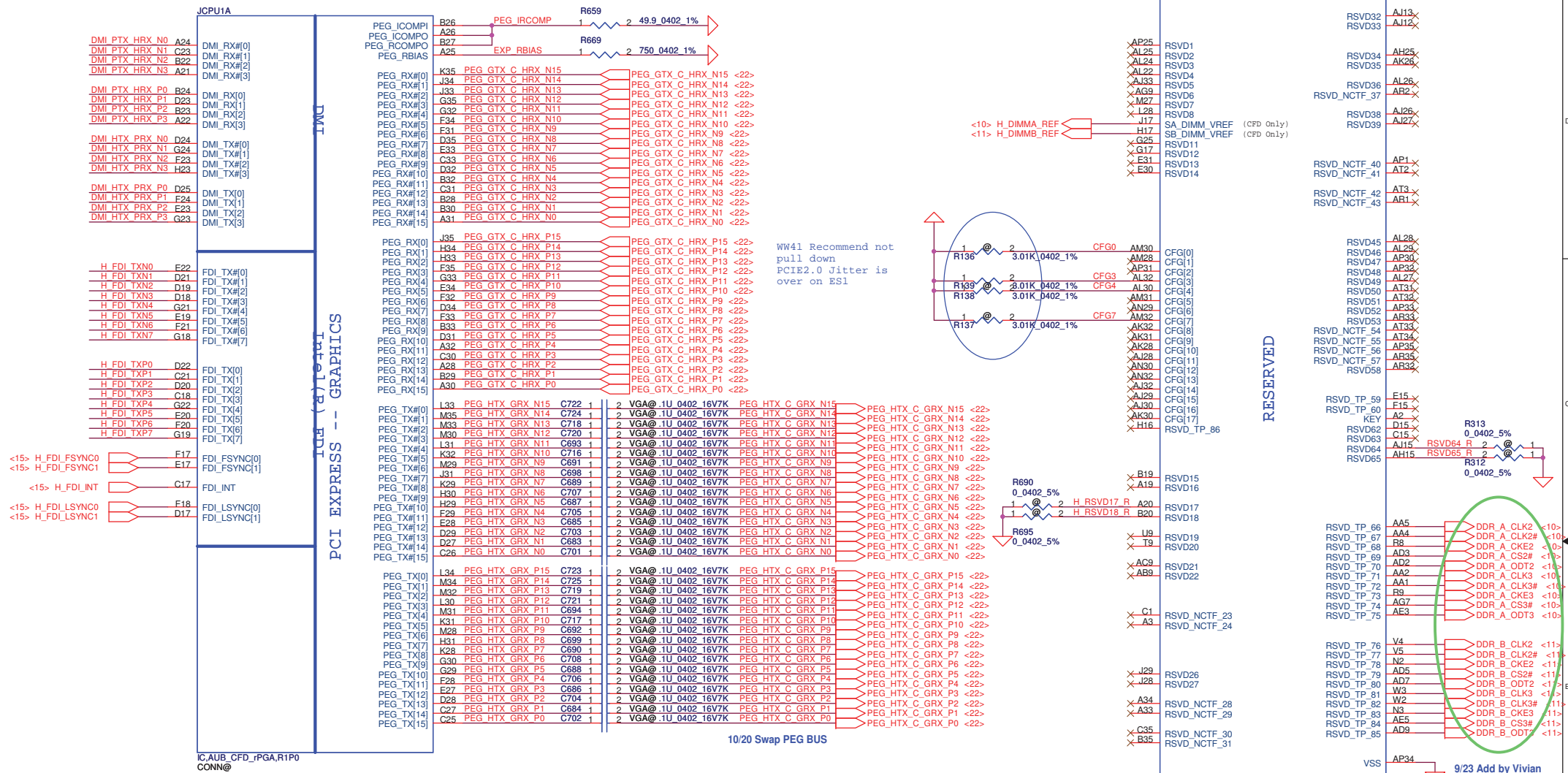
Board ID	PCB Revision
★ 0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Item	BOM Structure
DIS Only	DIS@
DGPU	VGA@
Broadway	WAY@
Madison	MAD@
Park	PAR@
Switchable Graphics	SG@

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB/B
	UHCI1	2	eSATA USB
		3	CMOS Camera
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	
		13	

Switchable Graphics (PARK) SKU: SG@/VGA@/PAR@
Switchable Graphics (MADISON) SKU: SG@/VGA@/MAD@
DIS ONLY (BROADWAY): DIS@/VGA@/WAY@

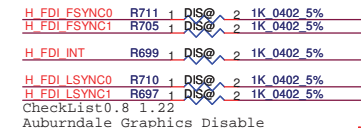
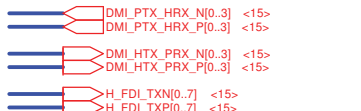
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eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG HTX_C_GRX_P15	PEG HTX_C_GRX_P0
eDP_TX#0	PEG HTX_C_GRX_N15	PEG HTX_C_GRX_N0
eDP_TX1	PEG HTX_C_GRX_P14	PEG HTX_C_GRX_P1
eDP_TX#1	PEG HTX_C_GRX_N14	PEG HTX_C_GRX_N1
eDP_TX2	PEG HTX_C_GRX_P13	PEG HTX_C_GRX_P2
eDP_TX#2	PEG HTX_C_GRX_N13	PEG HTX_C_GRX_N2
eDP_TX3	PEG HTX_C_GRX_P12	PEG HTX_C_GRX_P3
eDP_TX#3	PEG HTX_C_GRX_N12	PEG HTX_C_GRX_N3
eDP_AUX	PEG GTX_C_HRX_P13	PEG GTX_C_HRX_P2
eDP_AUX#	PEG GTX_C_HRX_N13	PEG GTX_C_HRX_N2

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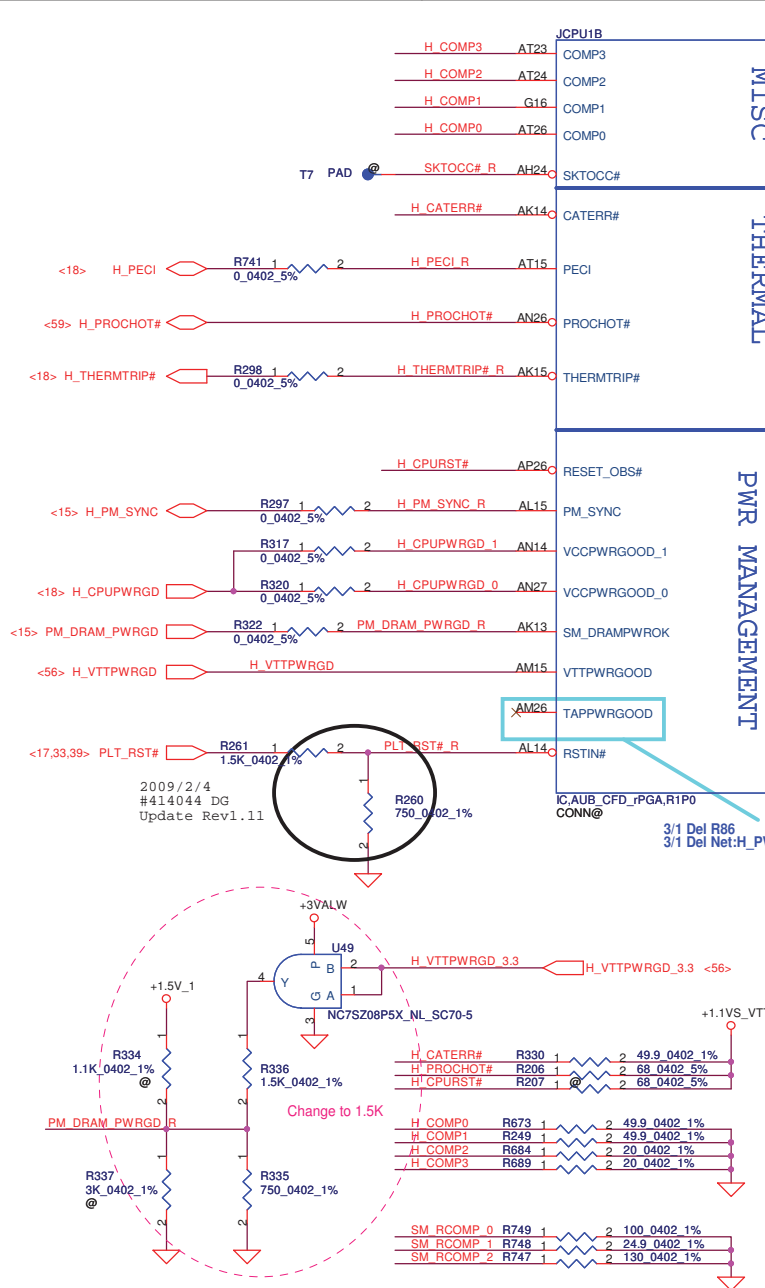
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CFG0 - PCI-Express Configuration Select
*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal
*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

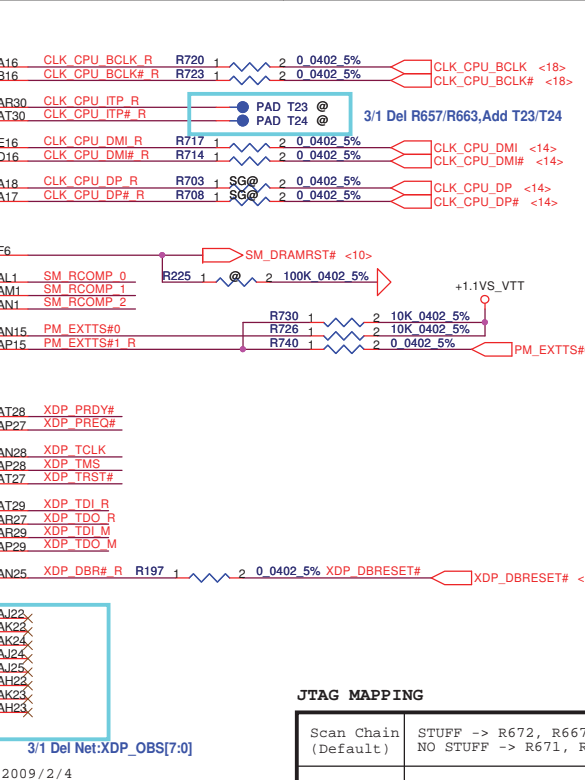
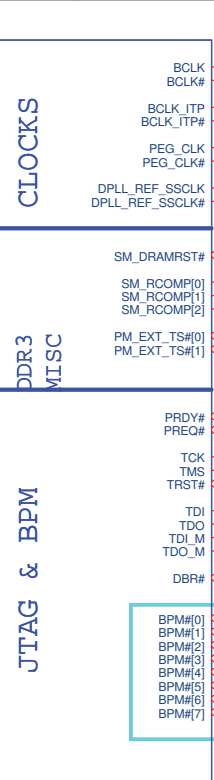
CFG4 - Display Port Presence
*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port
*:Default

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PROCESSOR (1/6) DMI,FDI,PEG			
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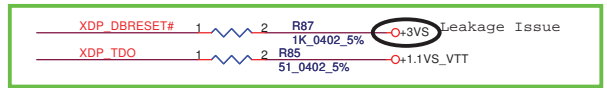
When implement S3 power reduction
not to pop R337
pop U49, R336, R335, R334...

2009/4/13
Intel Suggestion by Desige guide V1.52

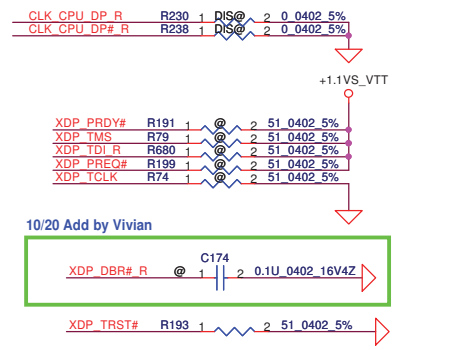


2009/2/4
Delete damping resistor for
power noise and Layout space
issue

3/1 Del JP5/R89/R92/R93/R96/C168



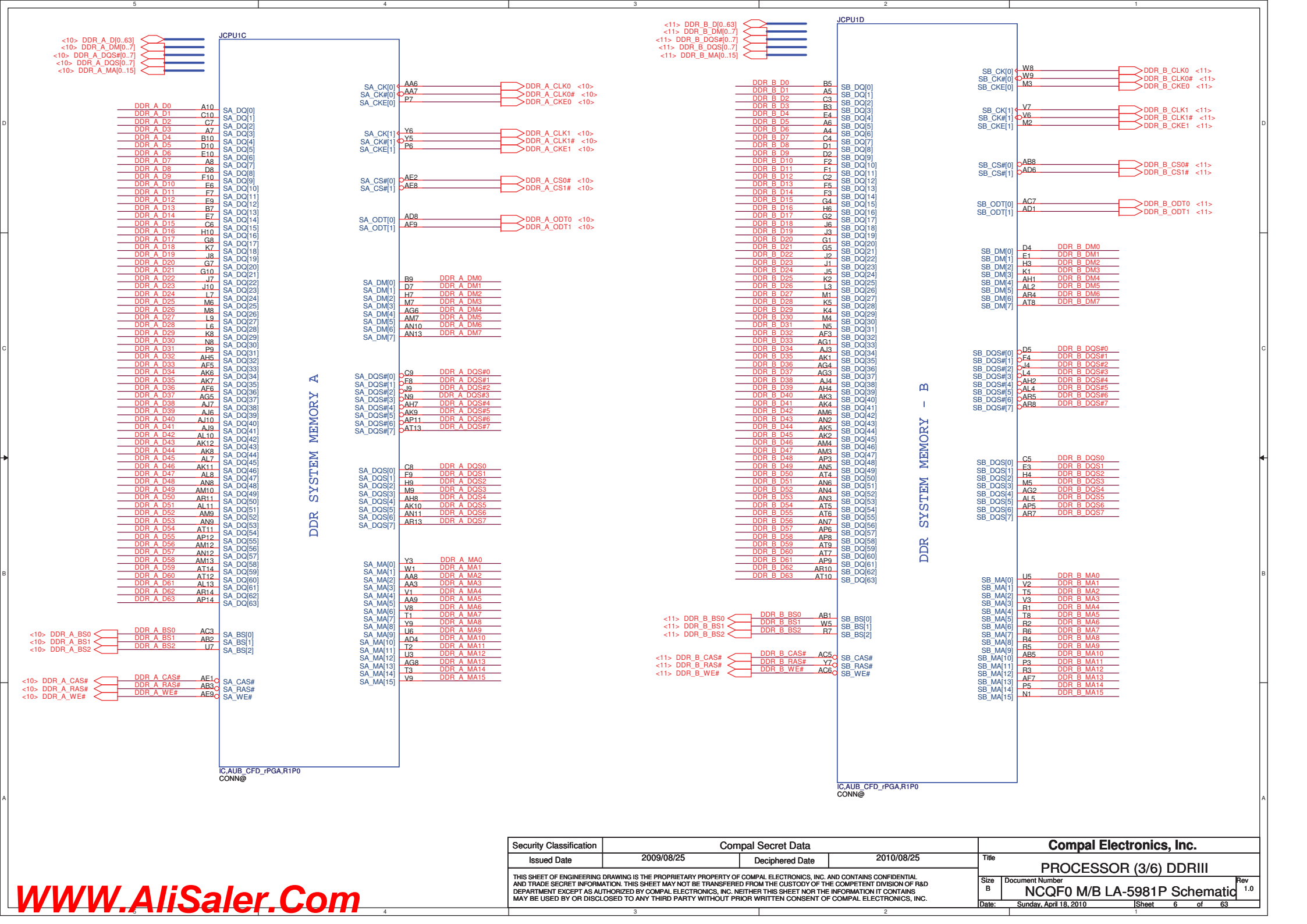
Processor CLK		
Reference Input Clock	Input Frequency	Associated PLL
BCLK/BCLK#	133MHz	Processor/Memory /Graphic
PEG_CLK/ PEG_CLK#	100MHz	PCI Express/ DMI/FDI
DPLL_REF_SSCLK/ DPLL_REF_SSCLK#	120MHz	Embedded Displayport

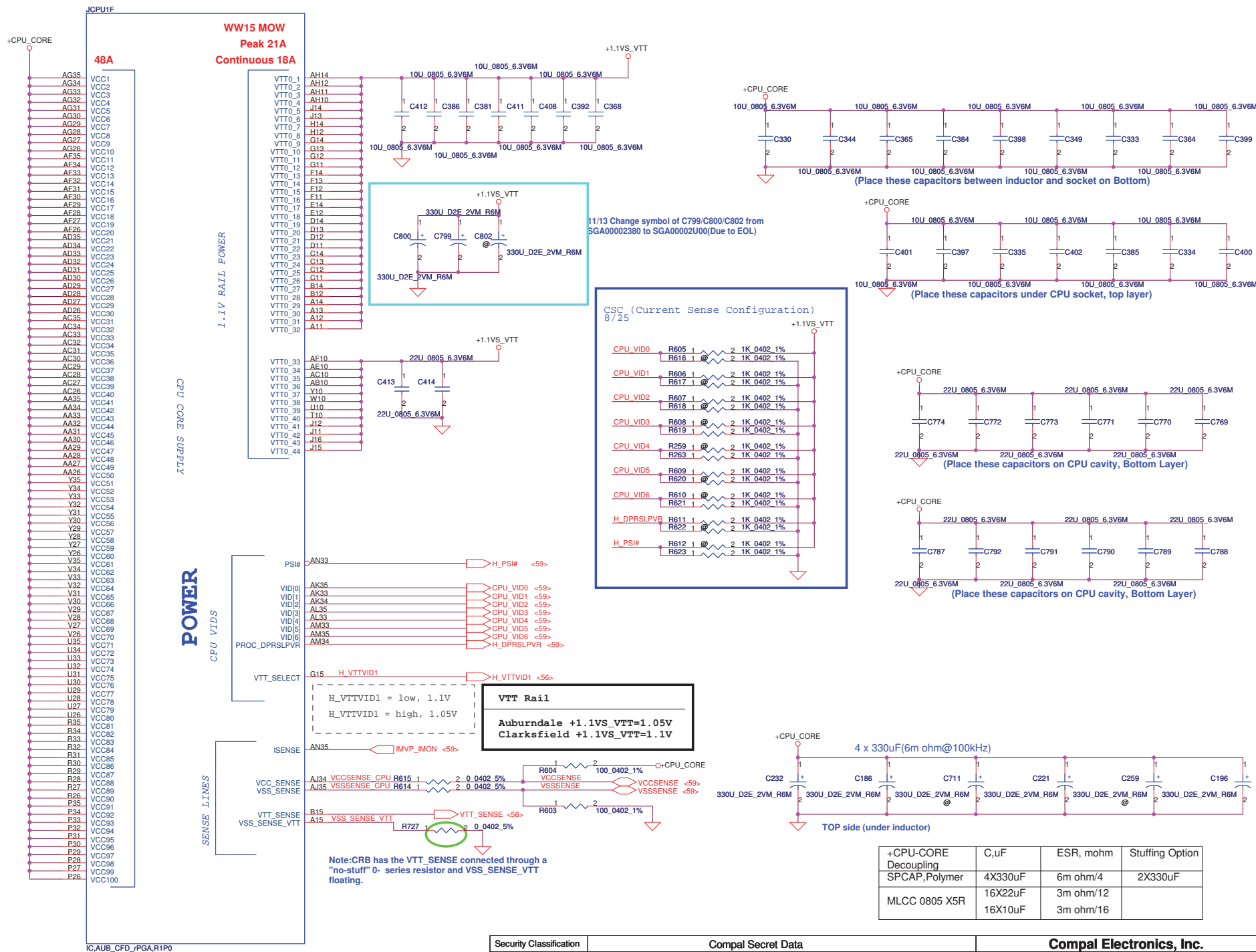


JTAG MAPPING

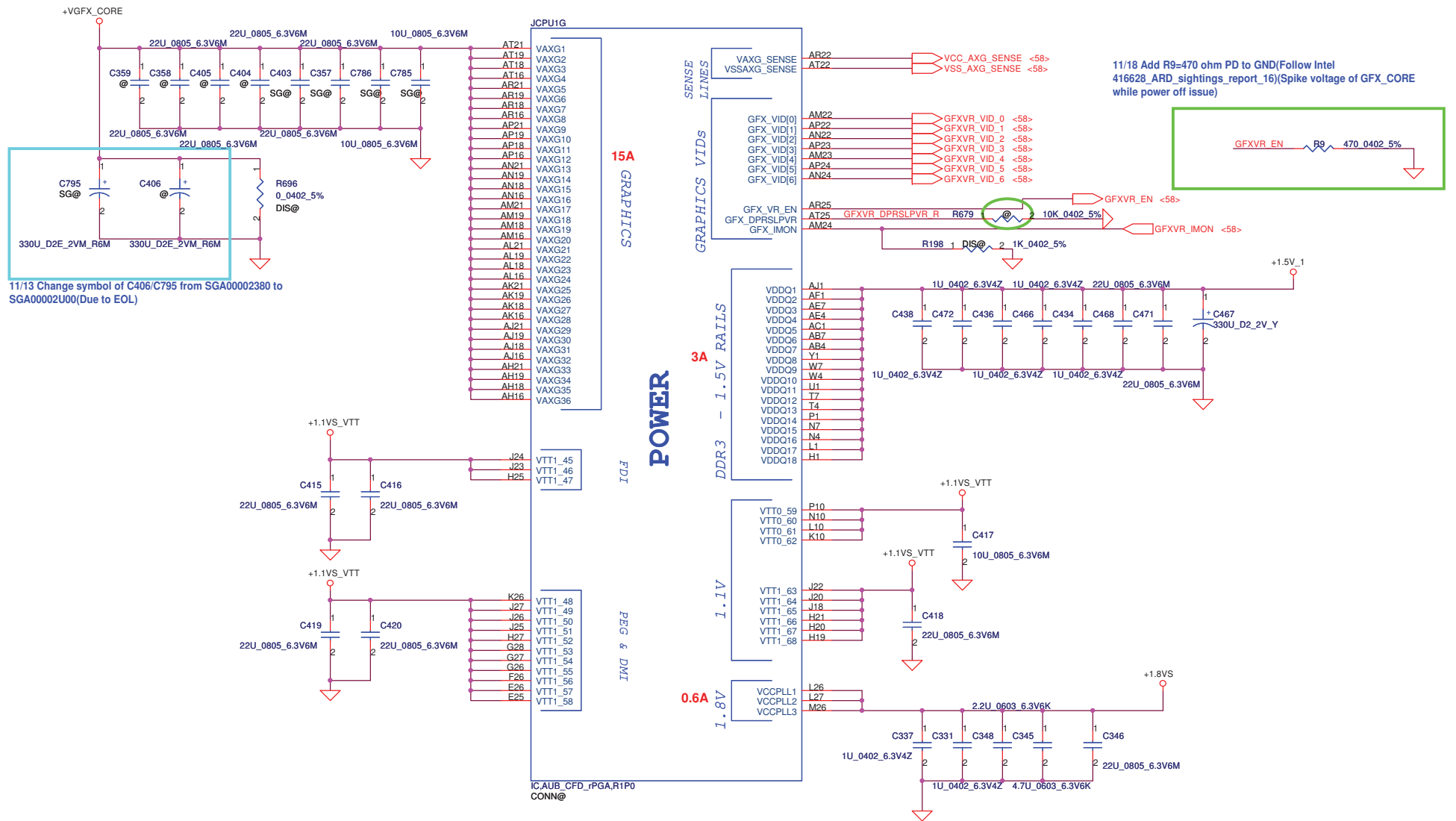
Scan Chain (Default)	STUFF -> R672, R667, R192 NO STUFF -> R671, R662
CPU Only	STUFF -> R672, R662 NO STUFF -> R667, R671, R192
GMCH Only	STUFF -> R671, R192 NO STUFF -> R672, R662, R667

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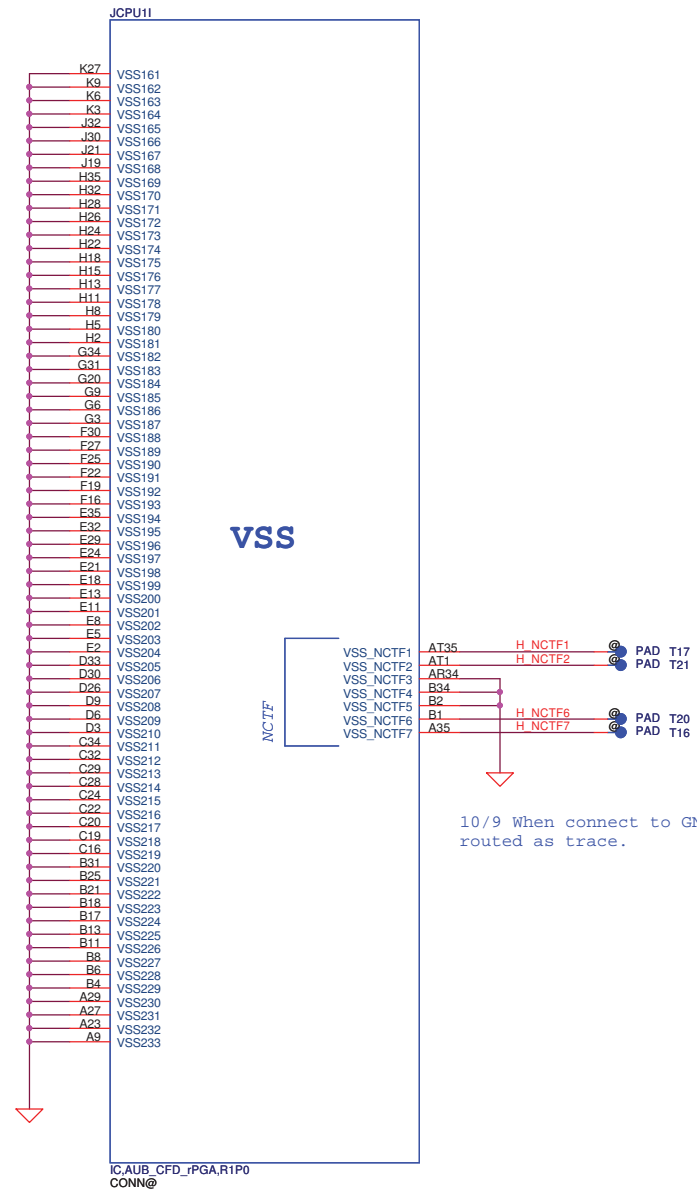
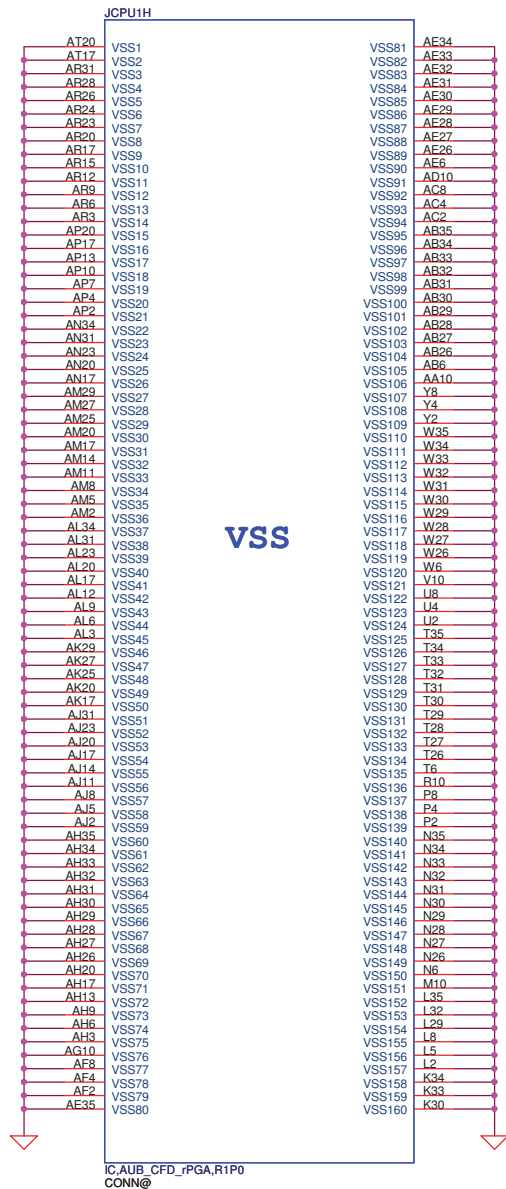




IC,AUB_CFD_PGA,R1P0
CONN@

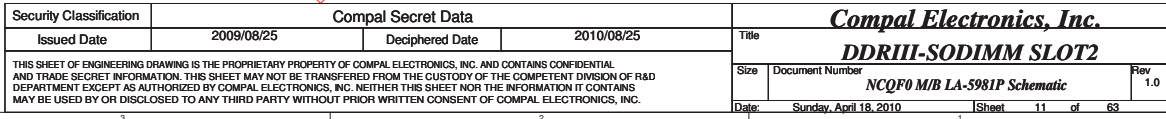


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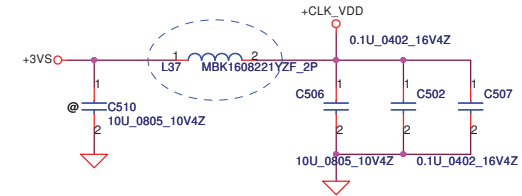
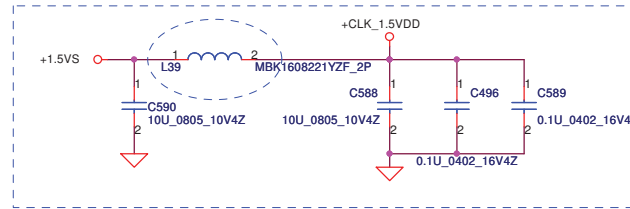
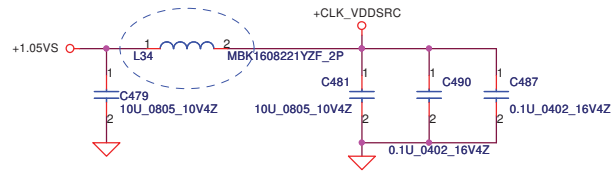
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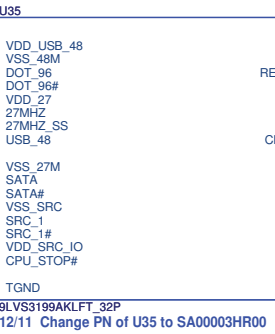
10/9 Change L34 part number
from SM010014520 to SM01000AX00

10/9 Change L39 part number
from SM010014520 to SM01000AX00

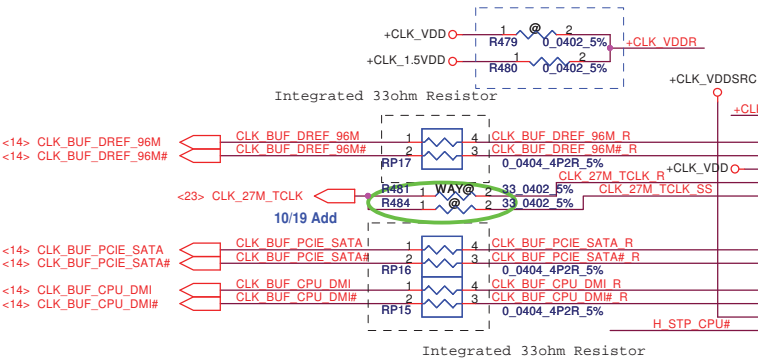


10/9 Change L37 part number
from SM010014520 to SM01000AX00

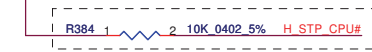
Clock Generator



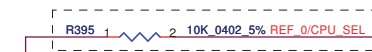
12/11 Change PN of U35 to SA00003HR00
LOW Power:
Realtek: RTM890N-631-VB-GRT, SA00003HQ10
*IDT: ICS9LVS3199AKLFT, SA00003HR00



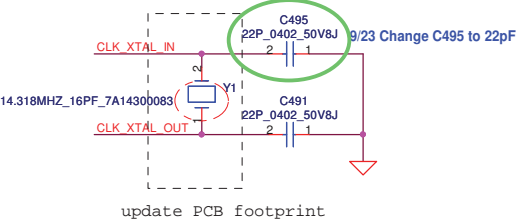
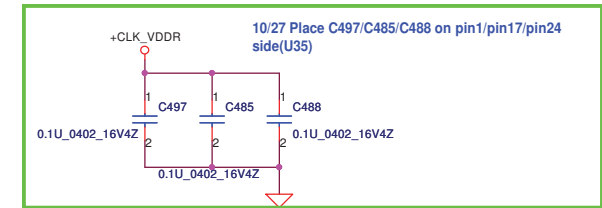
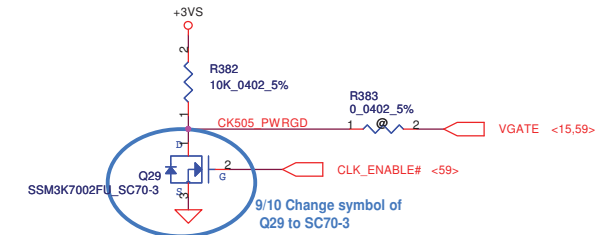
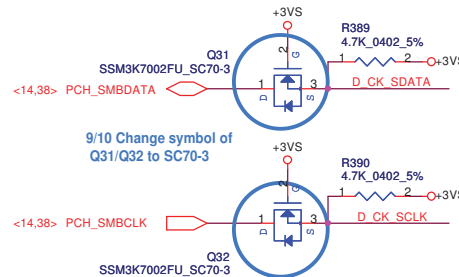
Silego Have Internal Pull-Up



IDT Have Internal Pull-Down



PIN	30	CPU_0	CPU_1
0 (Default)		133MHz	133MHz
1		100MHz	100MHz

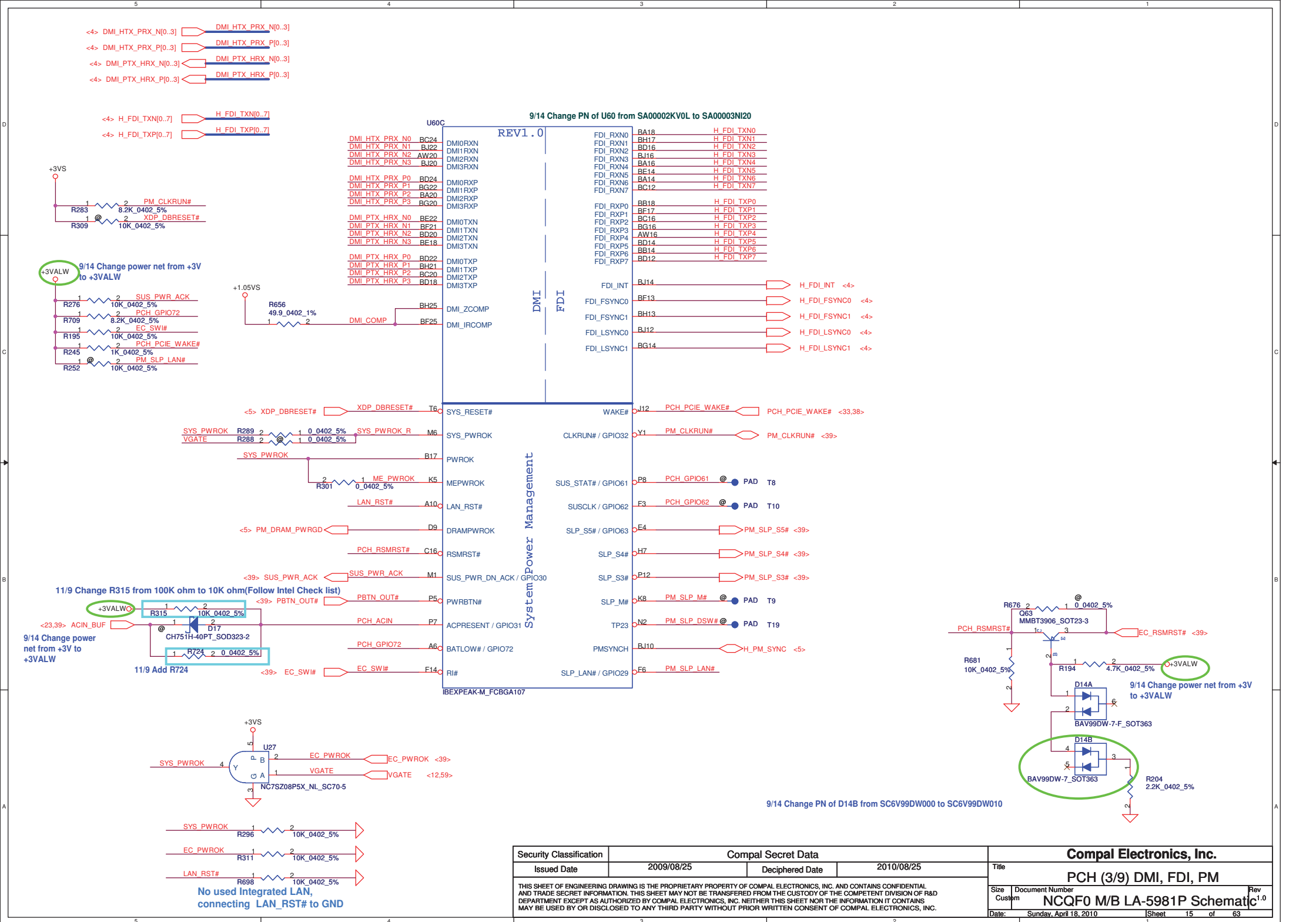


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								2010/08/25			
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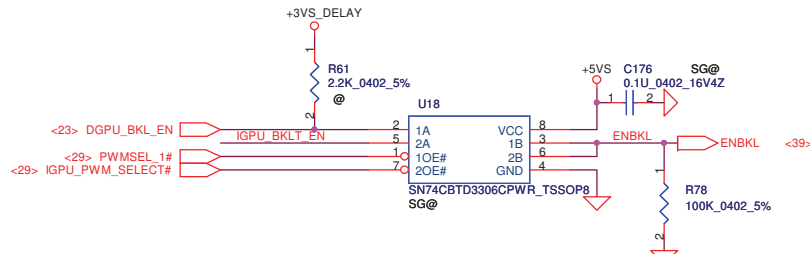
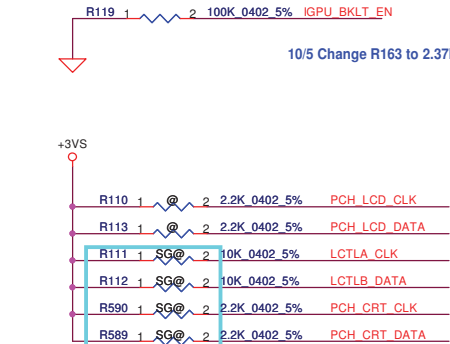
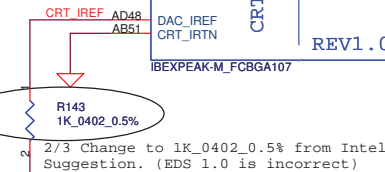
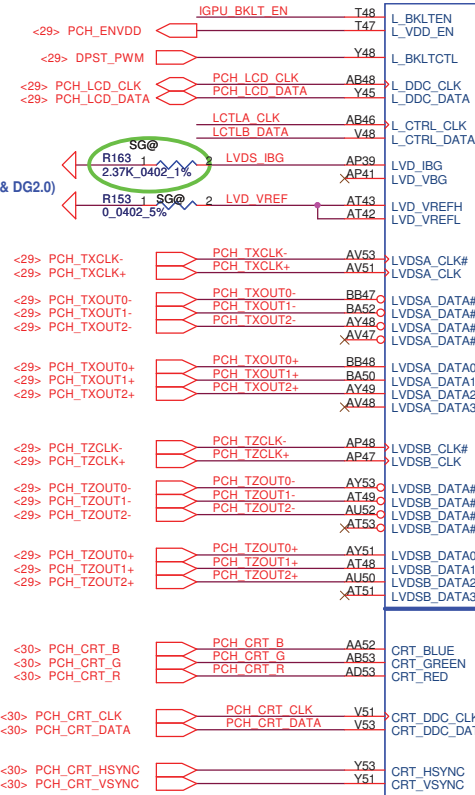
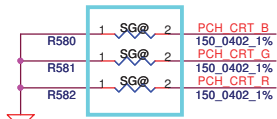
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12/11 Change Bom structure of R580/R581/R582/R111/R112/RR89/R590 from mount to SG@

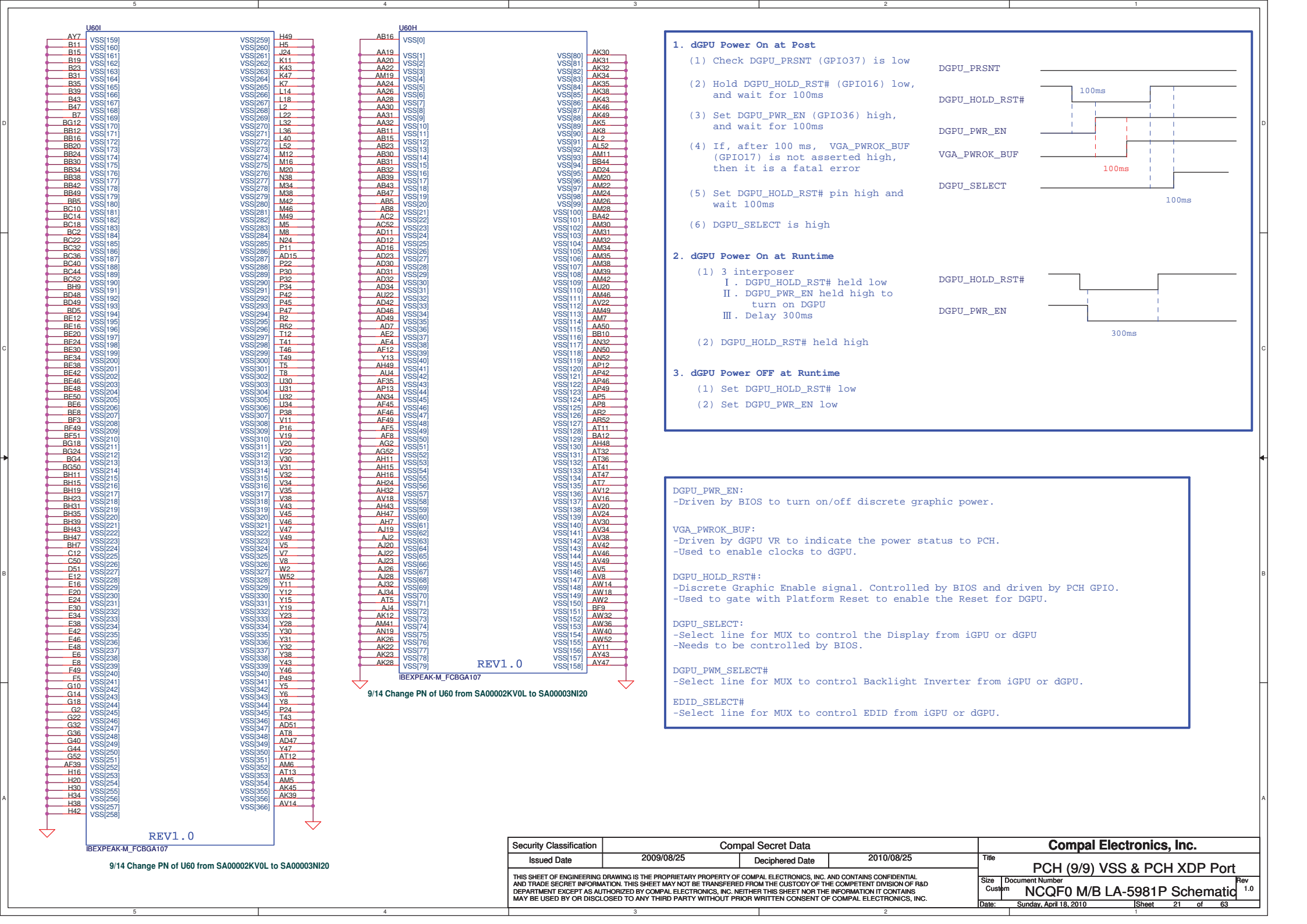


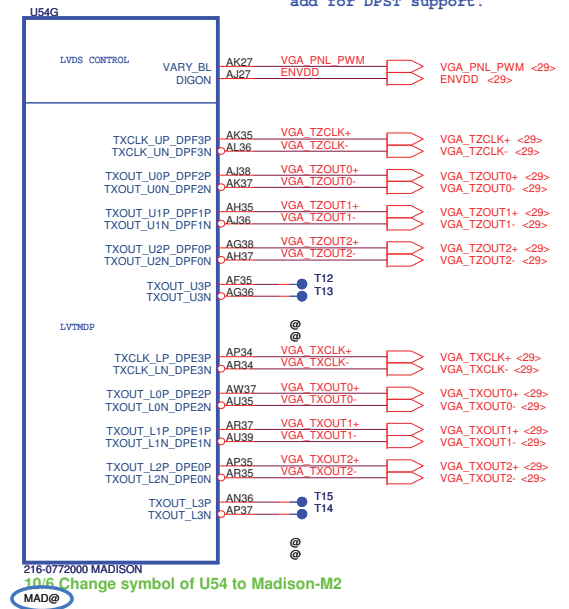
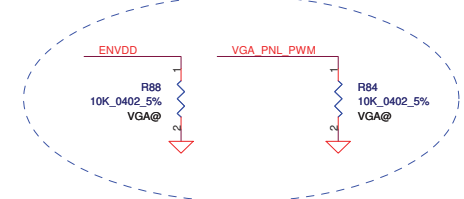
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9/14 Change poewr net to +1.0VSDGPU

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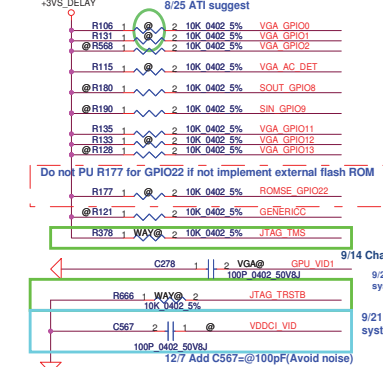
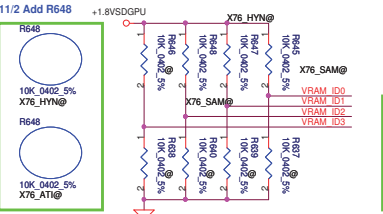
Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
CONFIG[1] CONFIG[2] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
SMS_EN_HARD	H2SYNC	Can be unconnected if not used.	0
VIP_DEVICE STRAP_DIS	V2SYNC	Can be unconnected if not used.	0

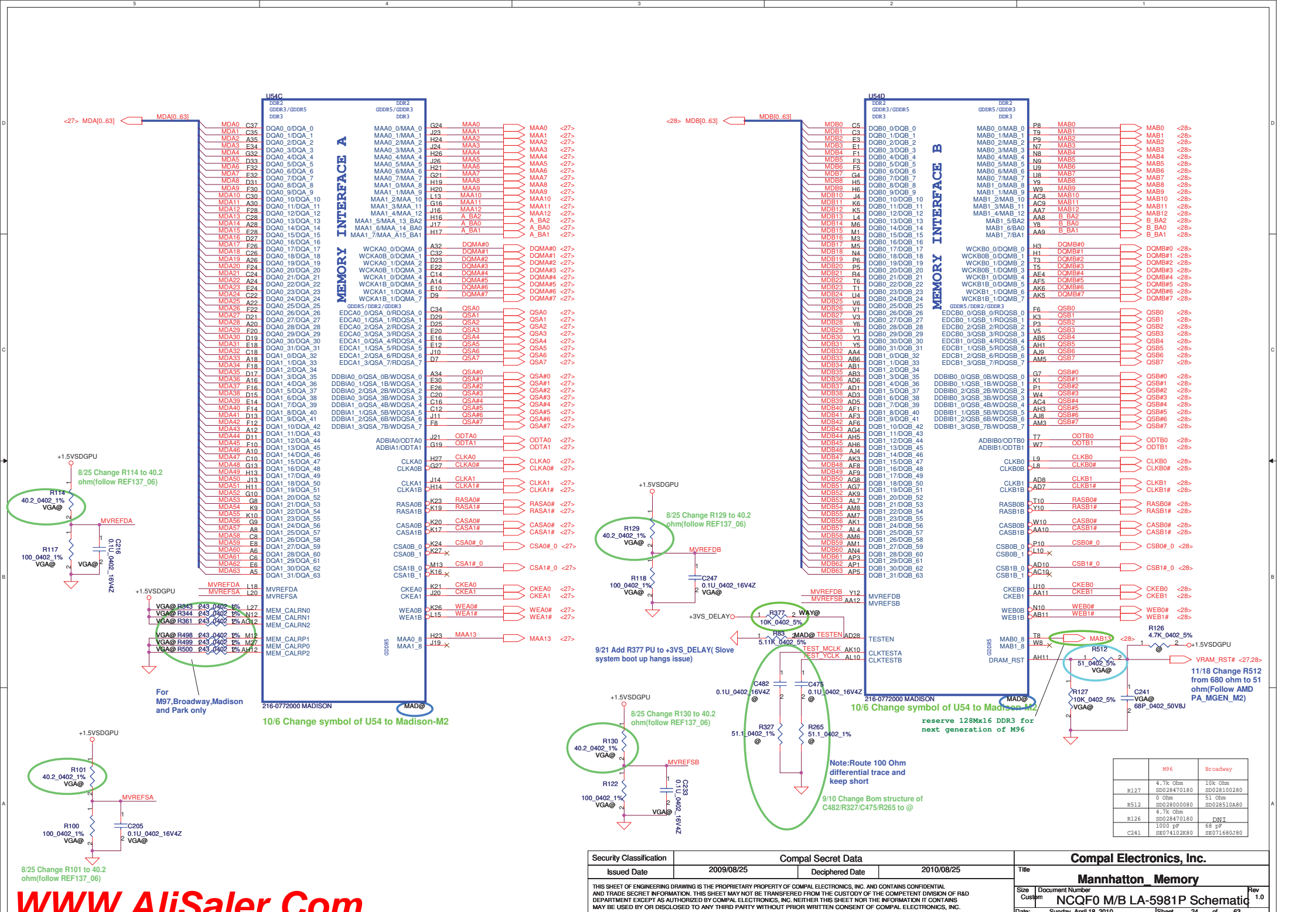
Madison Pro

Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
VRAM				
ATI(8pcs)1GB	0	1	0	0
Samsung(8pcs)1GB	0	1	0	1
Hynix(8pcs)1GB	0	1	1	0
Samsung(8pcs)128*16	1	1	0	1
Hynix(8pcs)128*16	1	1	1	0

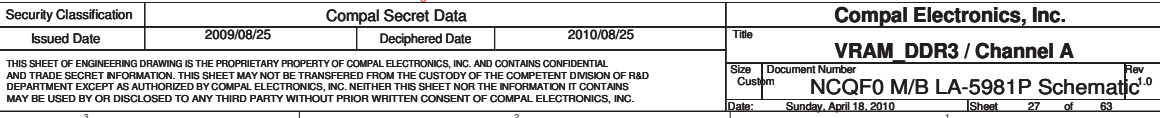
Broadway Pro

Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
VRAM				
ATI(8pcs)1GB	0	1	0	0
Samsung(8pcs)1GB	0	1	0	1
Hynix(8pcs)1GB	0	1	1	0
Samsung(8pcs)128*16	1	1	0	1
Hynix(8pcs)128*16	1	1	1	0



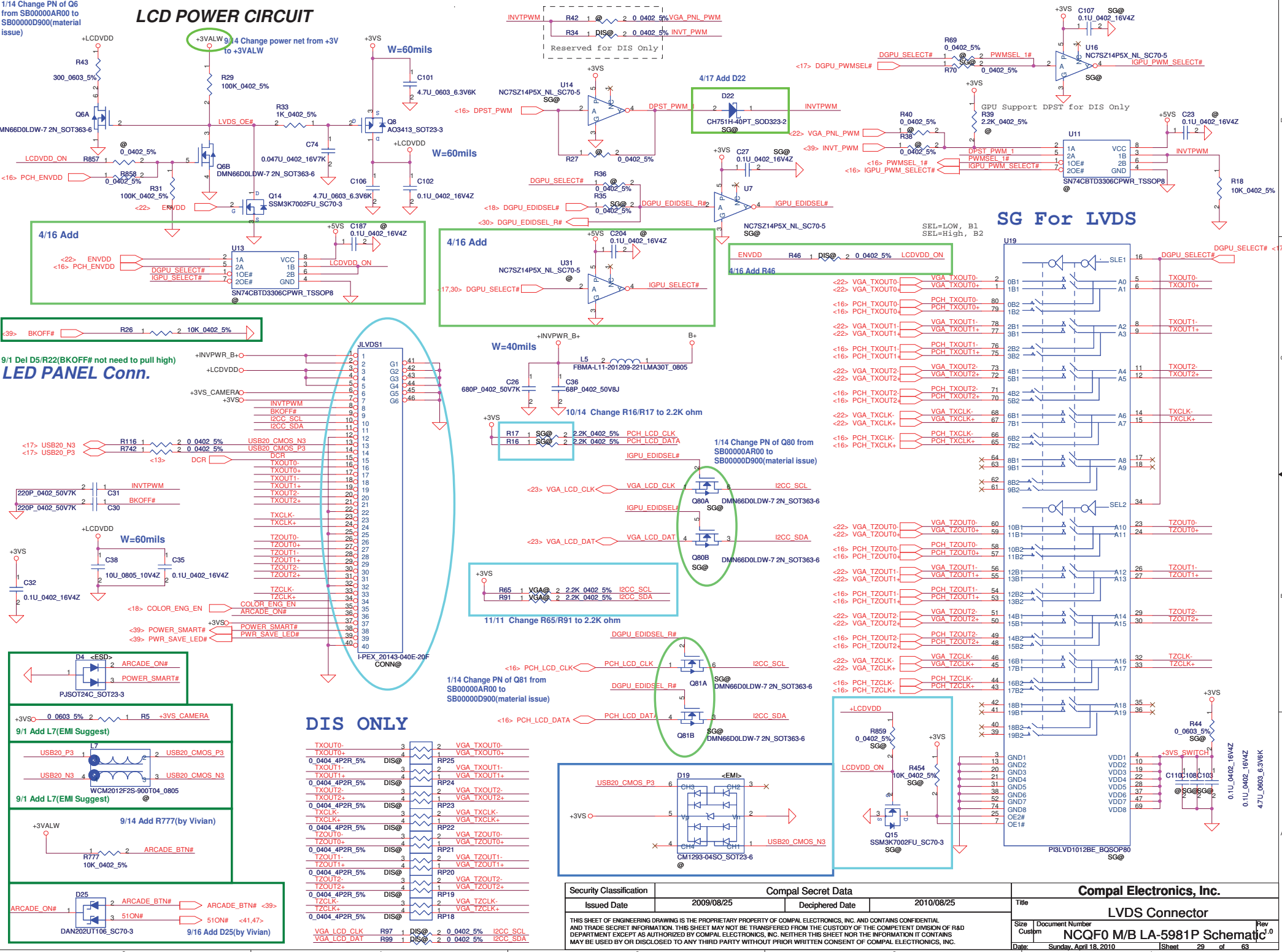








1/14 Change PN of Q6 from SB00000A000 to SB00000D900(material issue)



LCD POWER CIRCUIT

LED PANEL Conn.

DIS ONLY

SG For LVDS

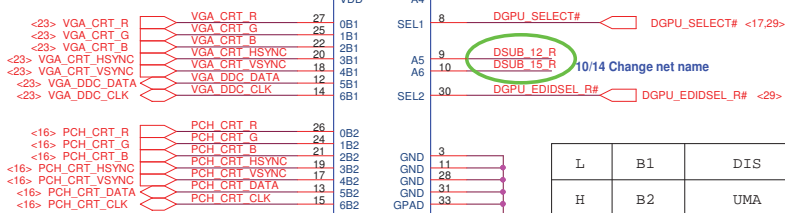
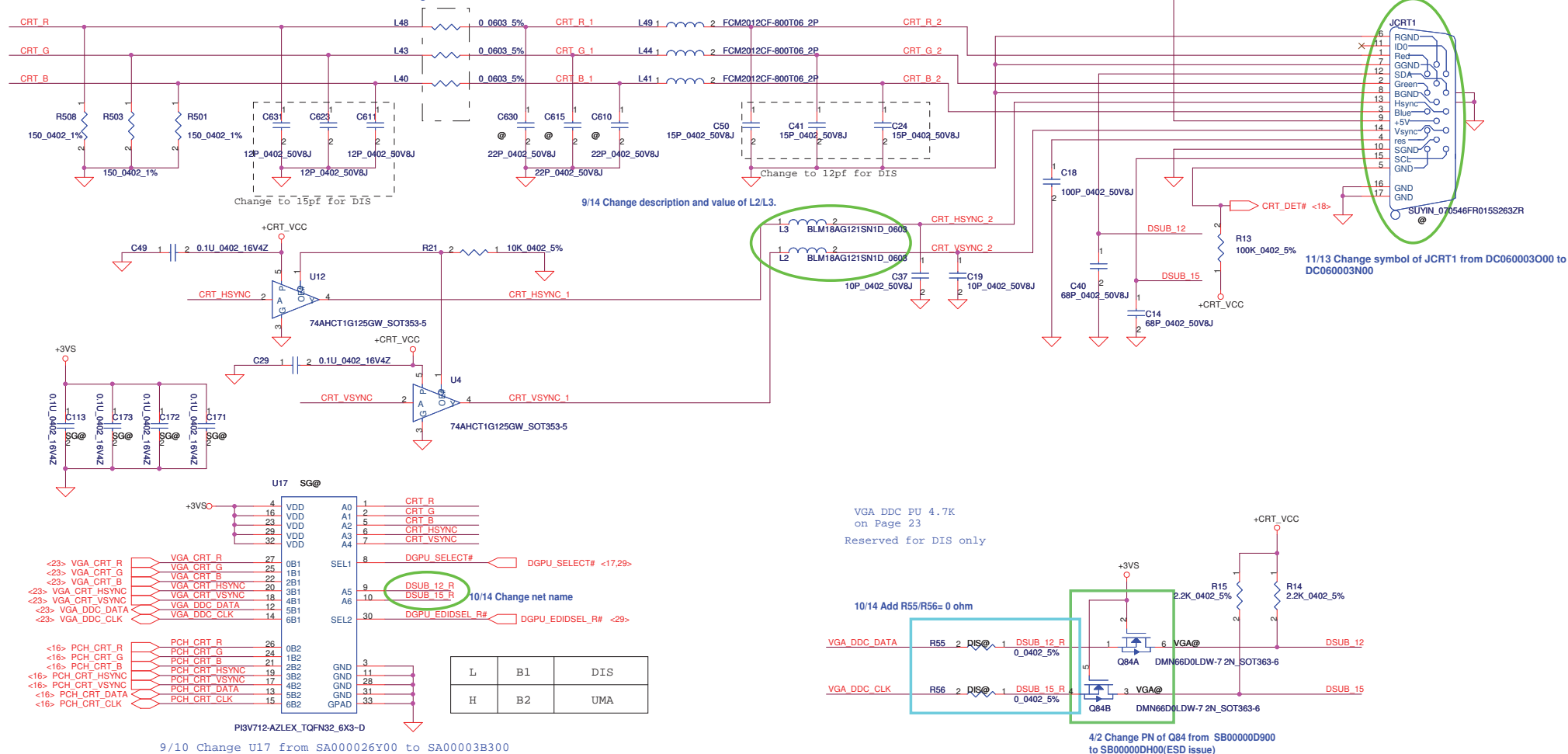
Security Classification		Compal Secret Data		Title	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	LVDS Connector	
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				Date Sunday, April 18, 2010	Sheet 29 of 63

CRT Connector

10/14 Change PN of L40/L43/L48 to SM01000AX00



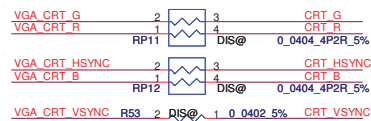
10/14 Change to 0 ohm for DIS



PI3V712-AZLEX_TOFN32_6X3-D

9/10 Change U17 from SA000026Y00 to SA00003B300
Michael

Reserved for DIS only

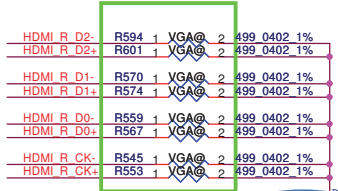


9/14 Change to RP for layout request
Michael

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				NCQF0 M/B LA-5981P Schematic	
				Date:	Rev
				Sunday, April 18, 2010	1.0
				Sheet	30 of 63

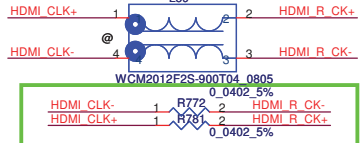
Place closed to JHDMI1

9/14 Change Bom structure from DIS @ to VGA@

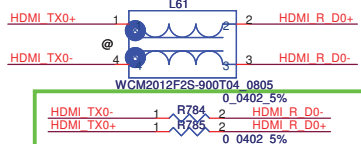


9/23 Change symbol of Q61 to SOT23-3

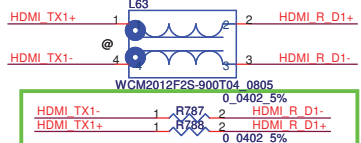
4/2 Change PN of Q61 from SB570020110 to SB000008J10



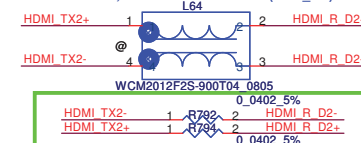
10/28 Del RP26, Add R772/R781=0 ohm(0402_5%)



10/28 Del RP27, Add R784/R785=0 ohm(0402_5%)

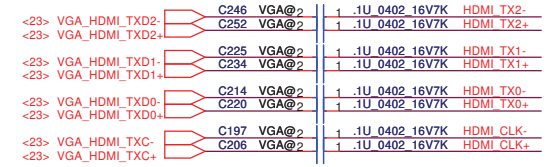


10/28 Del RP28, Add R787/R788=0 ohm(0402_5%)



10/28 Del RP29, Add R792/R794=0 ohm(0402_5%)

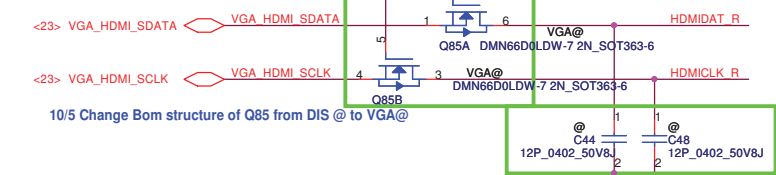
0914 Change to RP Michael



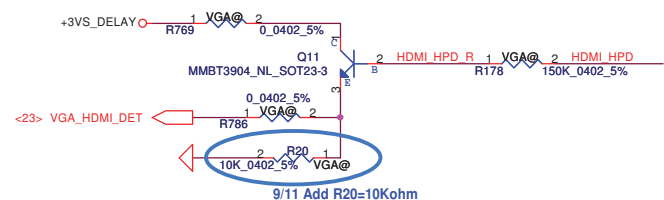
9/14 Add Q85(Bv Vivian)



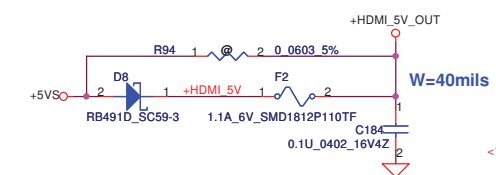
9/14 Change Bom structure of C44/C48 from DIS @ to @ 1/14 Change PN of Q85 from SB00000AR00 to SB00000D900(material issue)



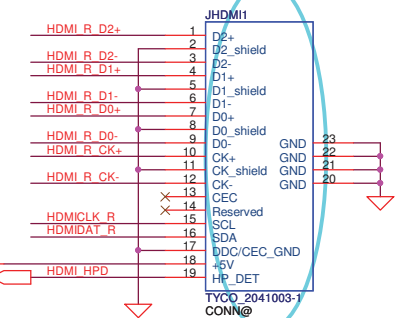
10/5 Change Bom structure of Q85 from DIS @ to VGA@



9/11 Add R20=10Kohm



9/14 Add R538/R544 by Vivian

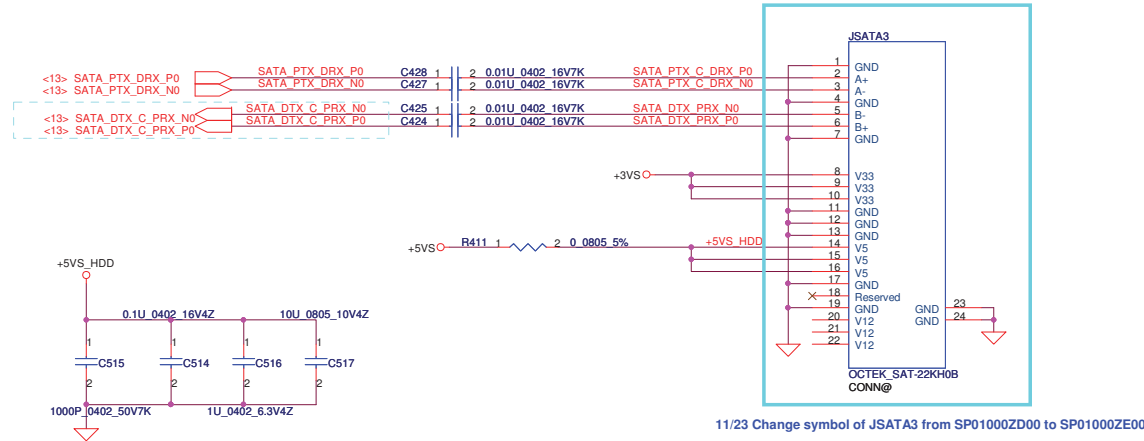


11/9 Change symbol of JHDMI1 from SP060003Z00 to DC232000A00

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Size	Custom	Document Number	NCQF0 M/B LA-5981P Schematic	Rev	1.0
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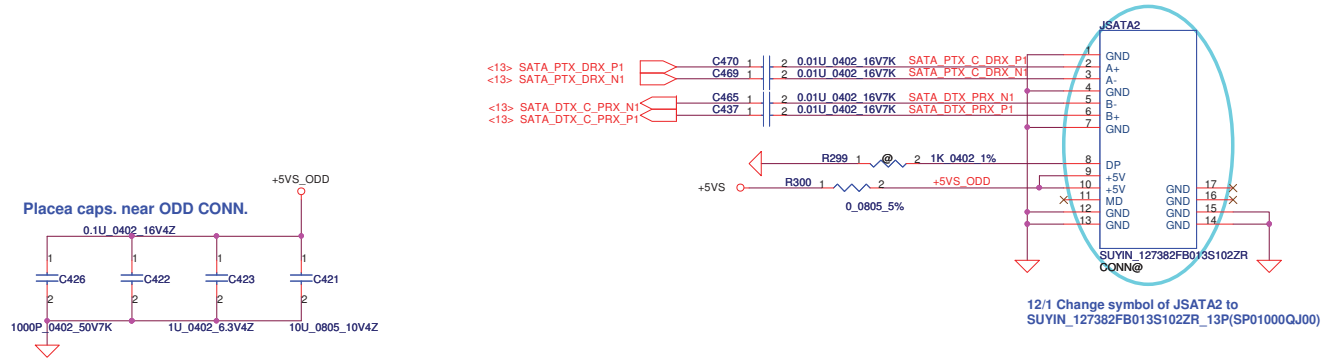
HDD

SATA HDD Conn.

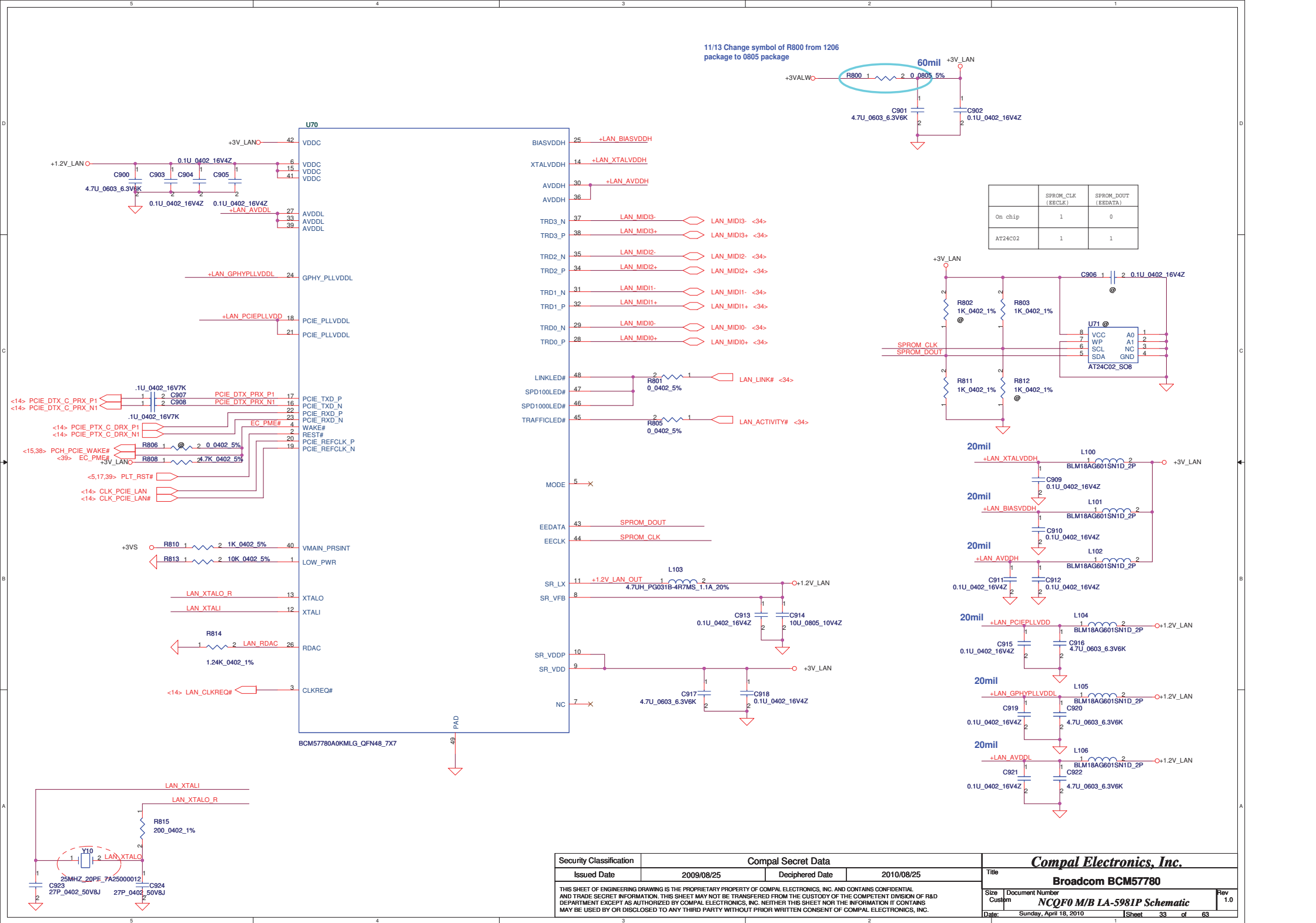


ODD

SATA ODD Conn.



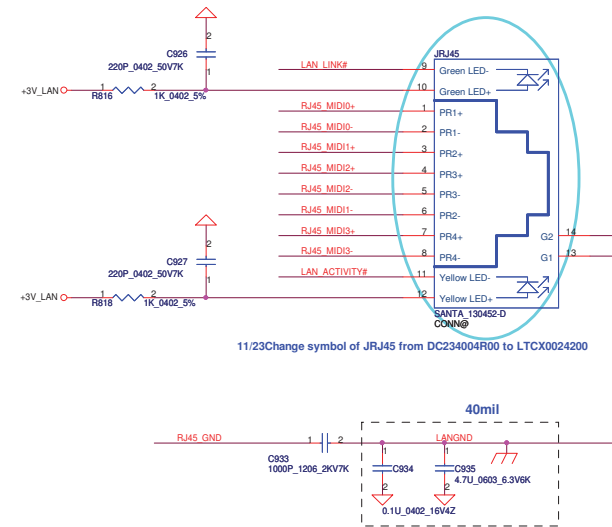
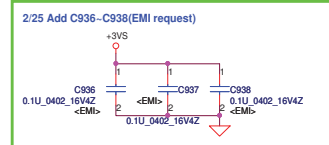
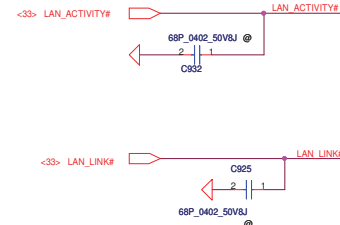
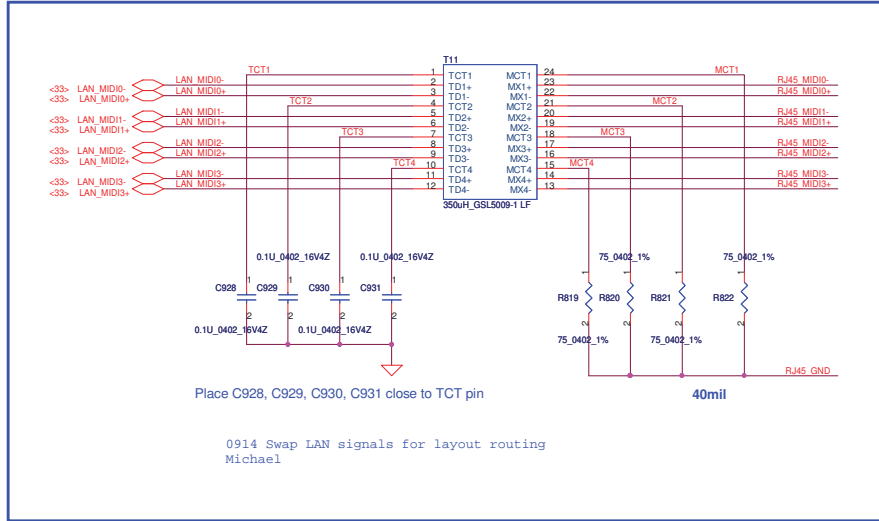
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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				Custom	NCQF0 M/B LA-5981P Schematic	1.0
				Date:	Sunday, April 18, 2010	Sheet 33 of 63

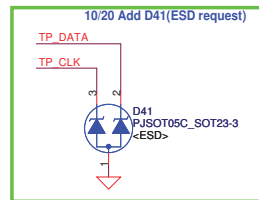
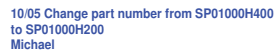
LAN Connector



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					NCQF0 M/B LA-5981P Schematic	1.0
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1/6 Add U37/R397/C503/C499=(ME request)

9/3 Change symbol of JTPB1 from ACES_85201-1605N to ACES_85201-1005N

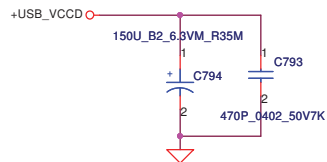


1/5 Change BOM Structure of R57/C228/1R1 from mount to CIR@

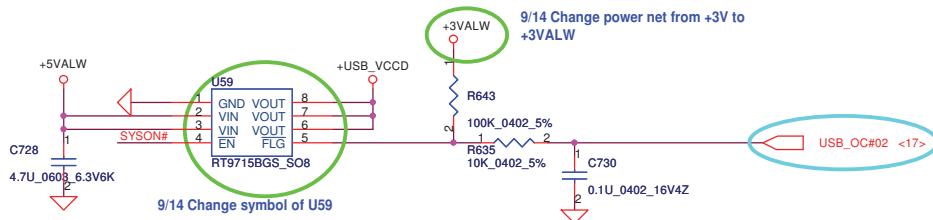
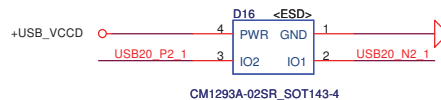
The diagram illustrates the replacement of three components (R57, C228, and 1R1) with a single CIR@ component. The circuit includes a +3VALW supply, a 100_0805_5% resistor (R57), a 4.7U_0805_10V4Z capacitor (C228), and an FM-2136SC-5CN chip. The CIR@ component is connected to the +3.3V_CIR supply, the RC1RRX signal, and the GND2GND1 ground. A red arrow points to the chip, indicating its replacement with CIR@.

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						1.0
				NCQ0 M/B LA-5981P Schematic		
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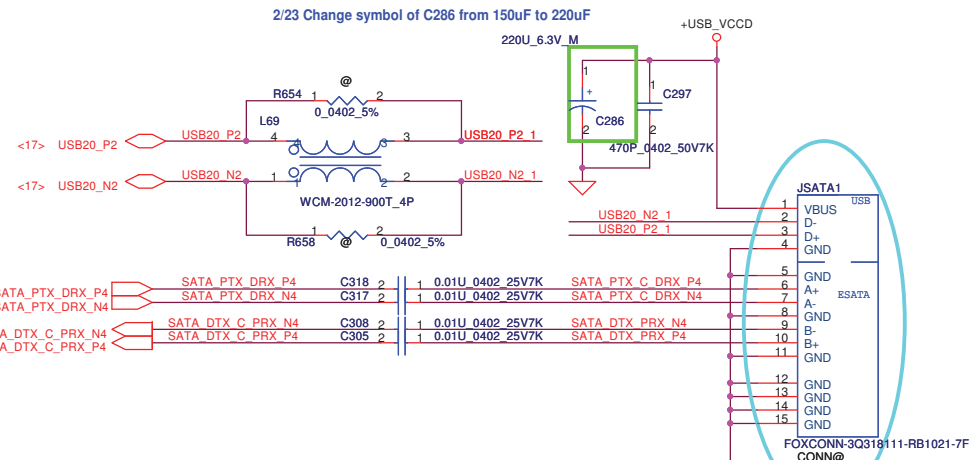
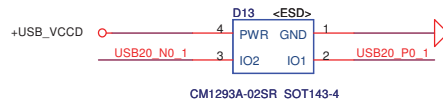
eSATA



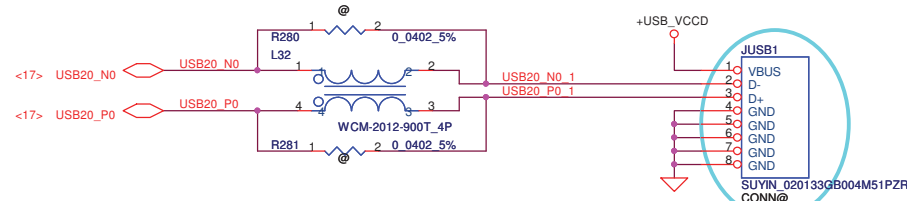
10/28 Add symbol of D16 of SC300000P00



10/28 Change symbol of D13 from SC300000000 to SC300000P00

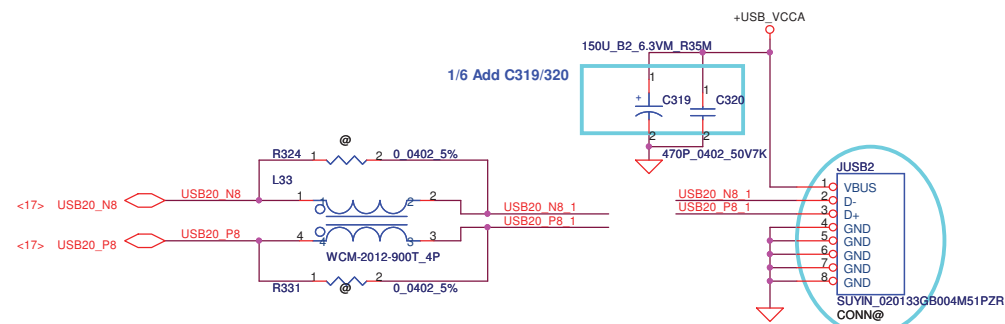
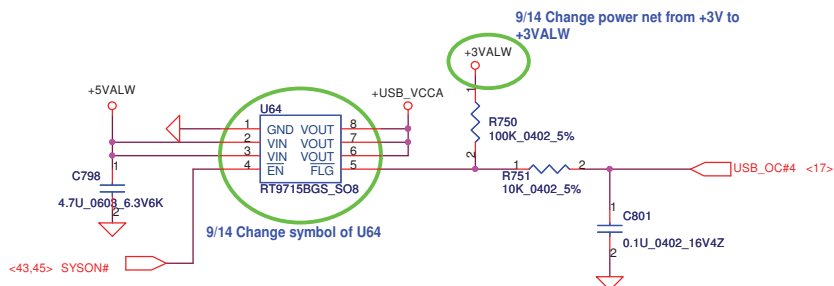


11/9 Change symbol of JSATA1 from DC230711060 to DC233004B00



11/9 Change symbol of JUSB1 from SP01000F100 to SP060004200

HS USB Port

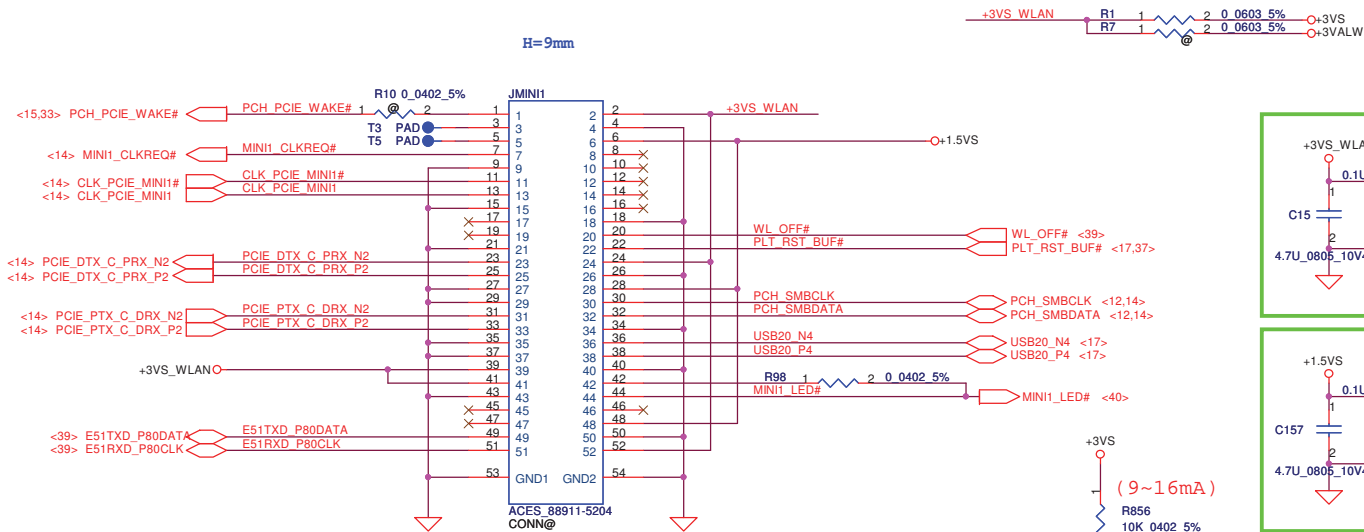


11/9 Change symbol of JUSB2 from SP01000B000 to SP060004200

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Size	Document Number	Rev		1.0	
Custom	NCQF0 M/B LA-5981P Schematic				
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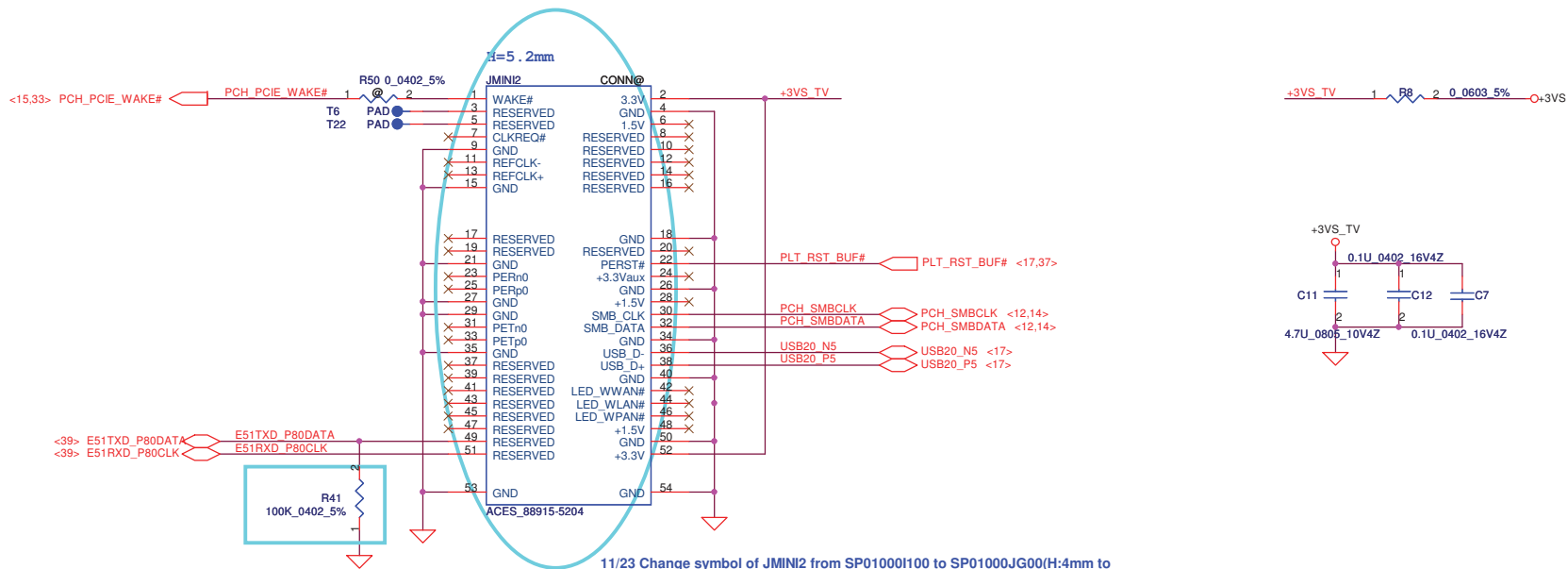
Compal Electronics, Inc.			
Title			
Card Reader JMB380			
Size	Document Number	R	
Custom	NCQF0 M/B LA-5981P Schematic		
Date:	Sunday, April 18, 2010	Sheet	37 of 63

WLAN



10/05 Change JMINI1 part number from SP01000I100 to SP01000FP00
Michael

MINI

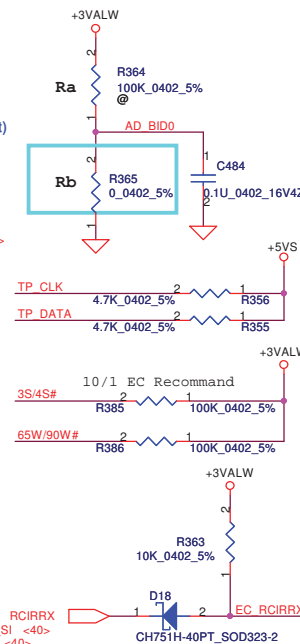
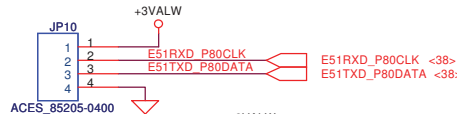


11/23 Change symbol of JMINI2 from SP01000I100 to SP01000JG00(H:4mm to H:5.2mm)

11/9 Change symbol of R41 from SD028100280 to SD028100380(10k ohm to 100k ohm)

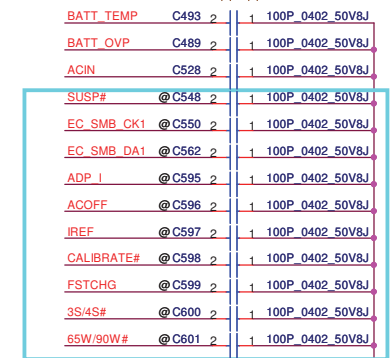
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	Rev		1.0	
Custom	NCQF0 M/B LA-5981P Schematic				
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For EC Tools



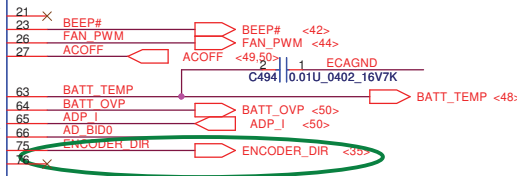
Analog Board ID definition, Please see page 3.

1/14 Change value of C518/C519 from 15pF to 18pF

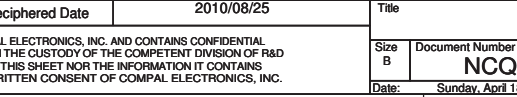
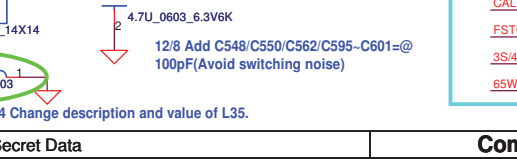
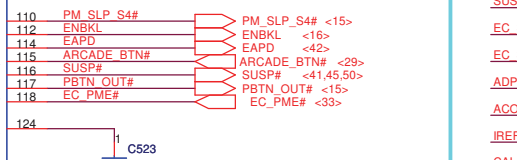
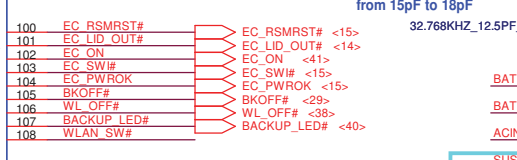
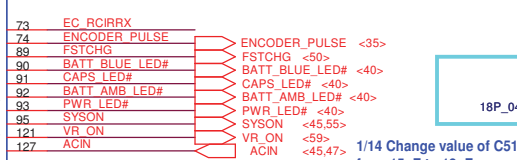
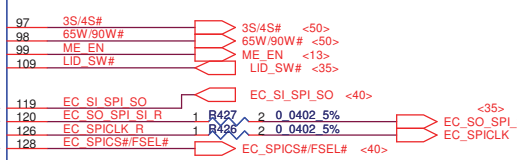
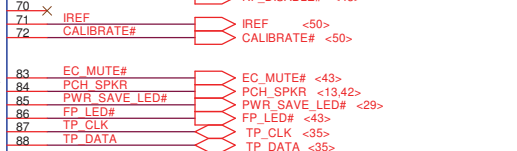


12/11 Change PN of U38 from SA00001J580 to SA00001J5A0(Rev:D3 to E0)

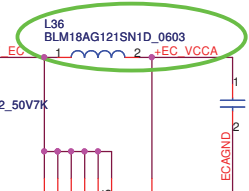
12/ 11 Change R365 from 100K to 0 ohm(Follow EC request)



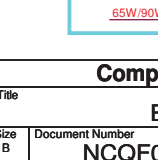
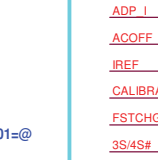
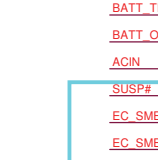
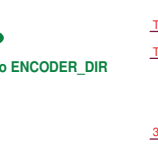
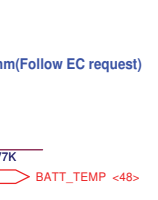
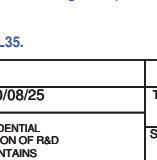
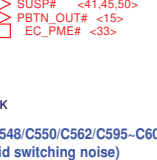
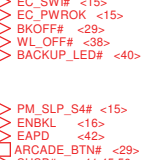
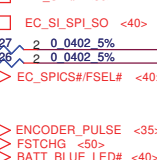
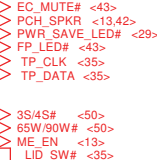
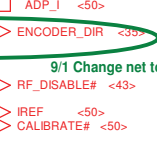
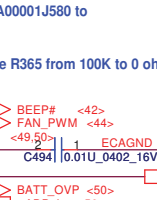
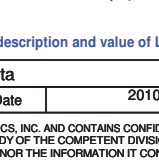
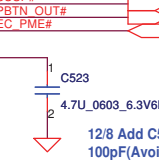
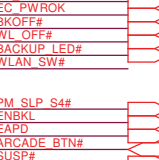
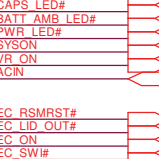
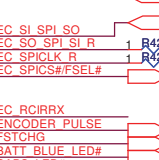
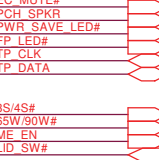
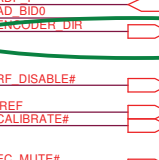
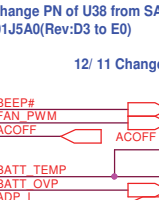
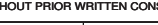
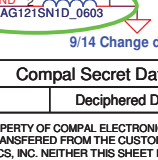
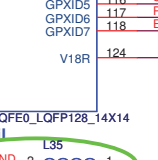
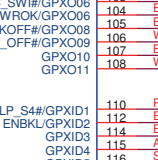
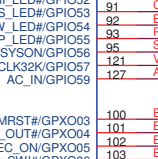
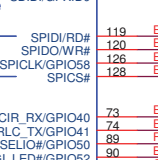
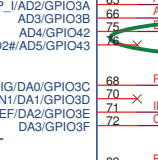
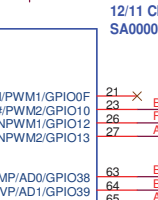
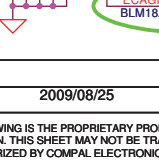
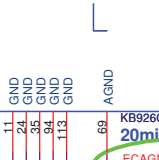
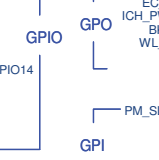
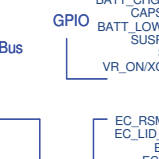
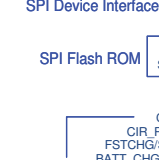
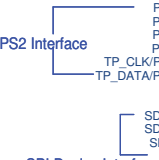
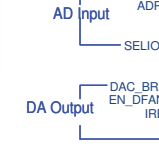
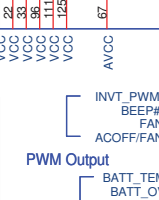
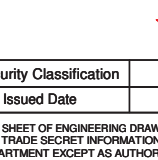
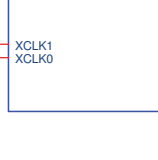
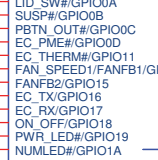
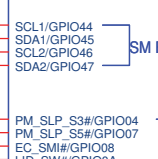
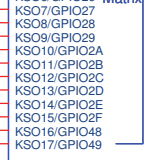
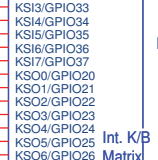
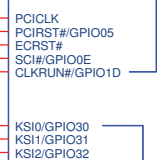
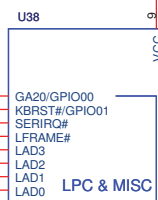
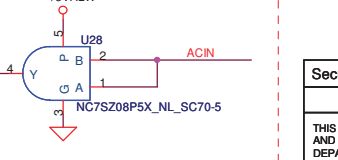
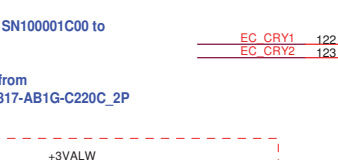
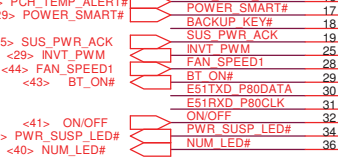
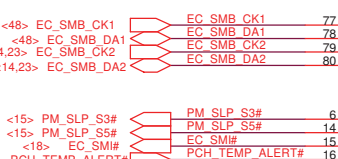
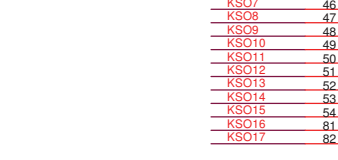
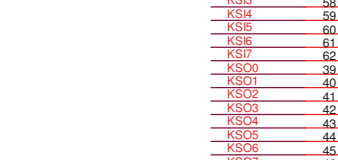
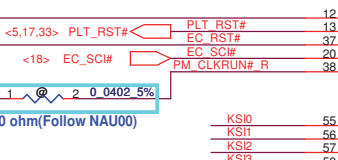
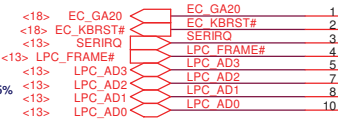
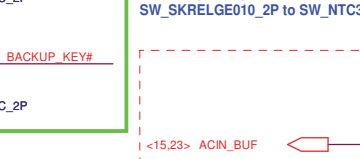
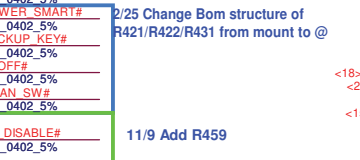
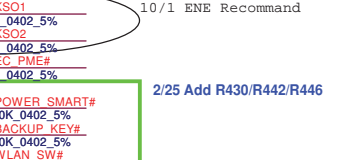
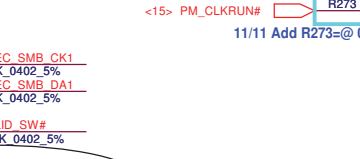
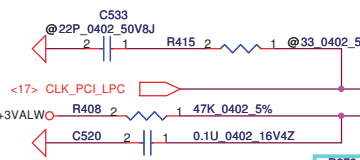
9/1 Change net to ENCODER_DIR



9/14 Change description and value of L36.

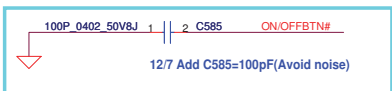
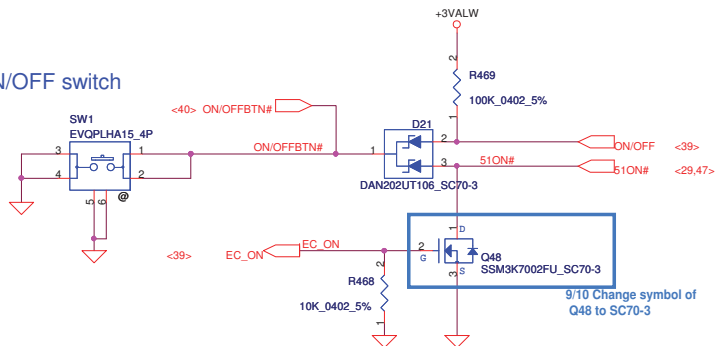


9/14 Add By Vivian(EMI suggest)

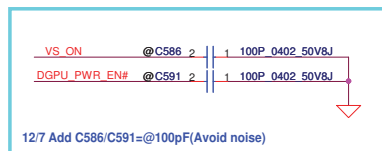
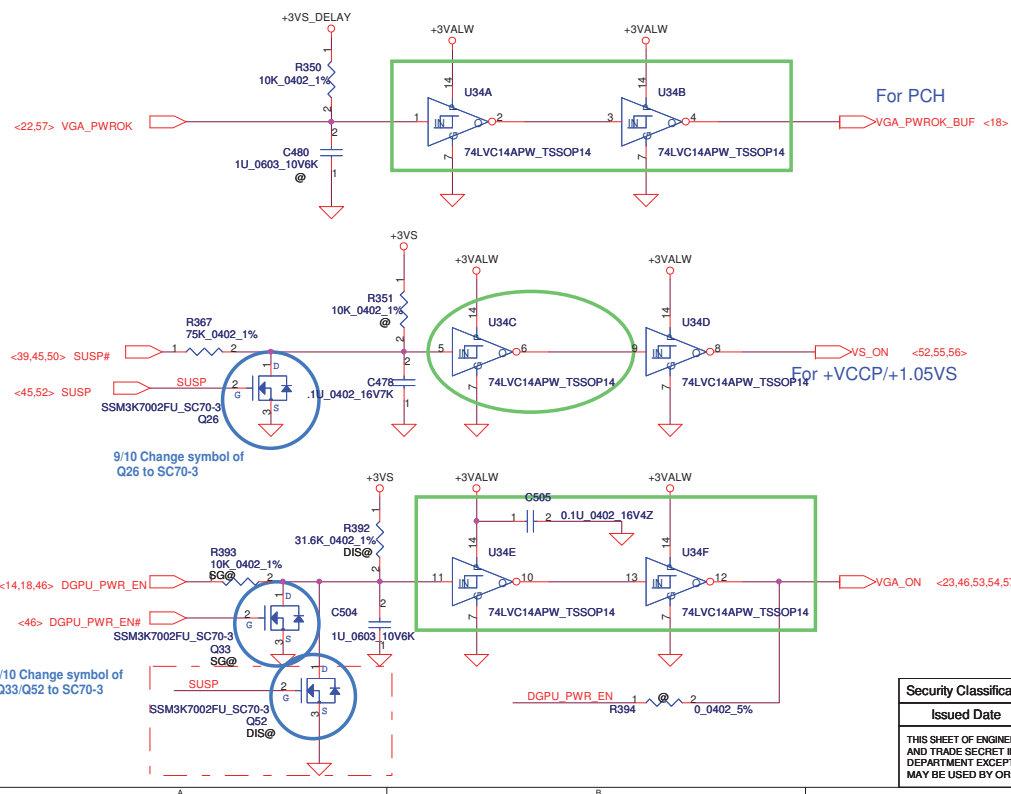


Power Button

ON/OFF switch

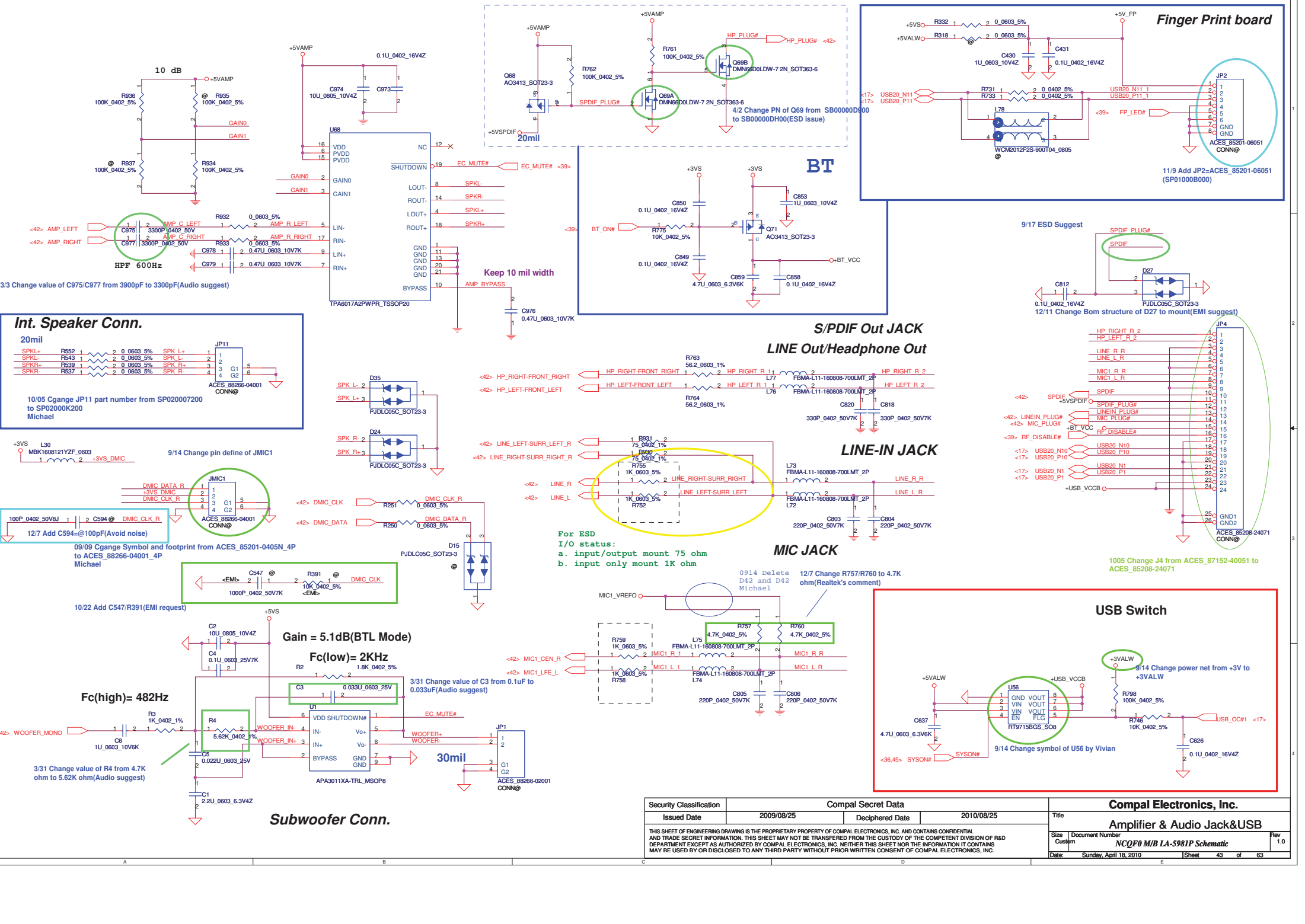


Power ON Circuit

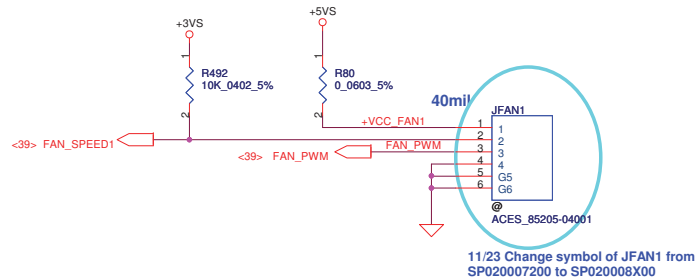


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Size B				Document Number				NCQF0 M/B LA-5981P Schematic			
Date				Sunday, April 18, 2010				Sheet 41 of 63			
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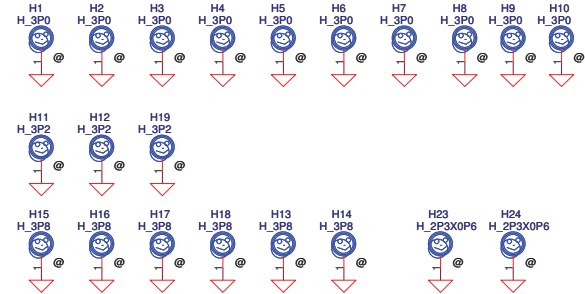
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FAN1 Conn



Screw



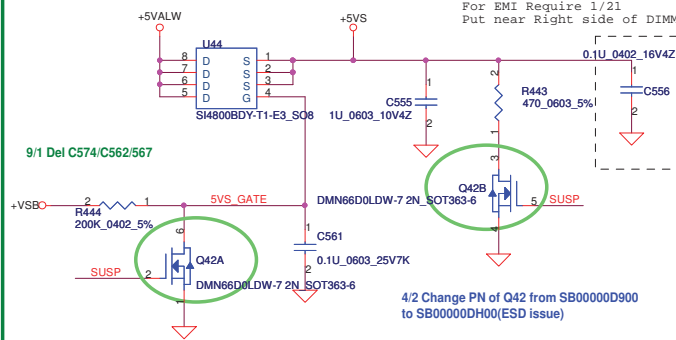
NON-PDH

2/25 Change footprint of H22

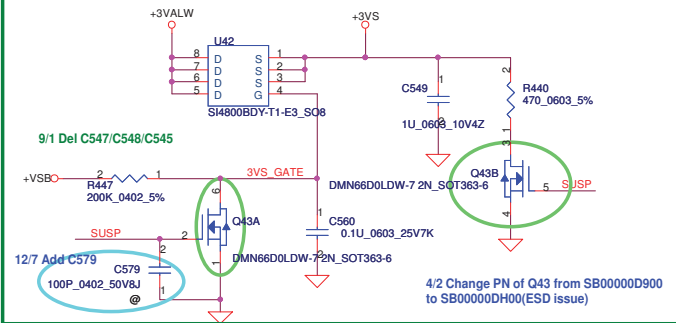


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				Date:	NCQF0 M/B LA-5981P Schematic
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+5VALW TO +5VS

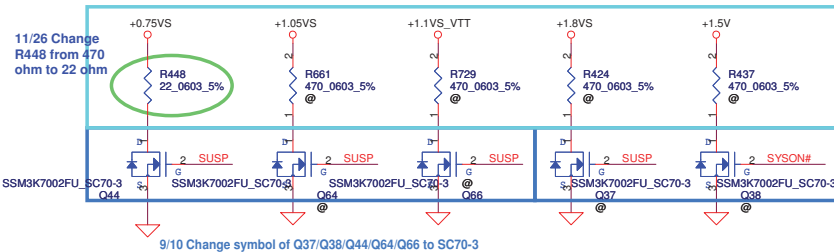
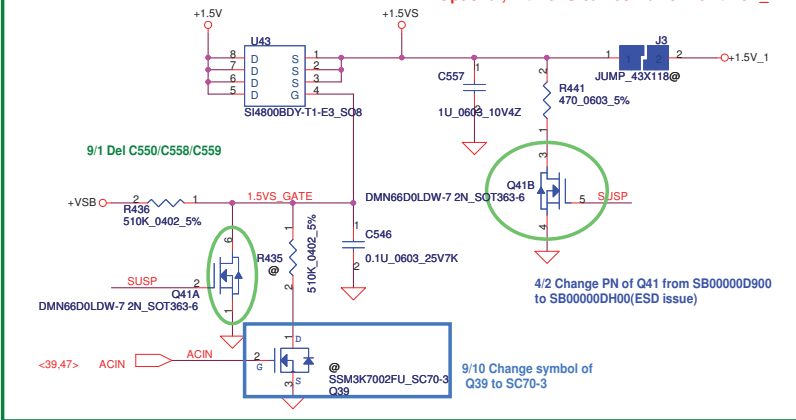


+3VALW TO +3VS

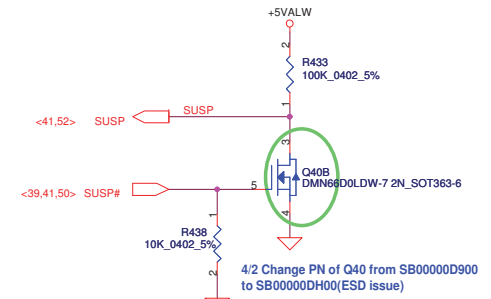
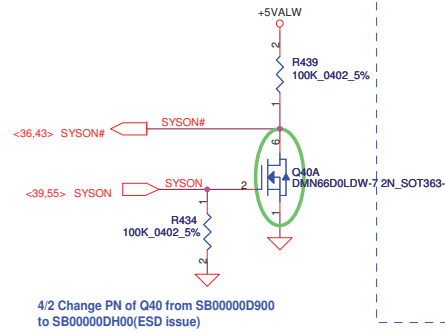


+1.5V to +1.5VS

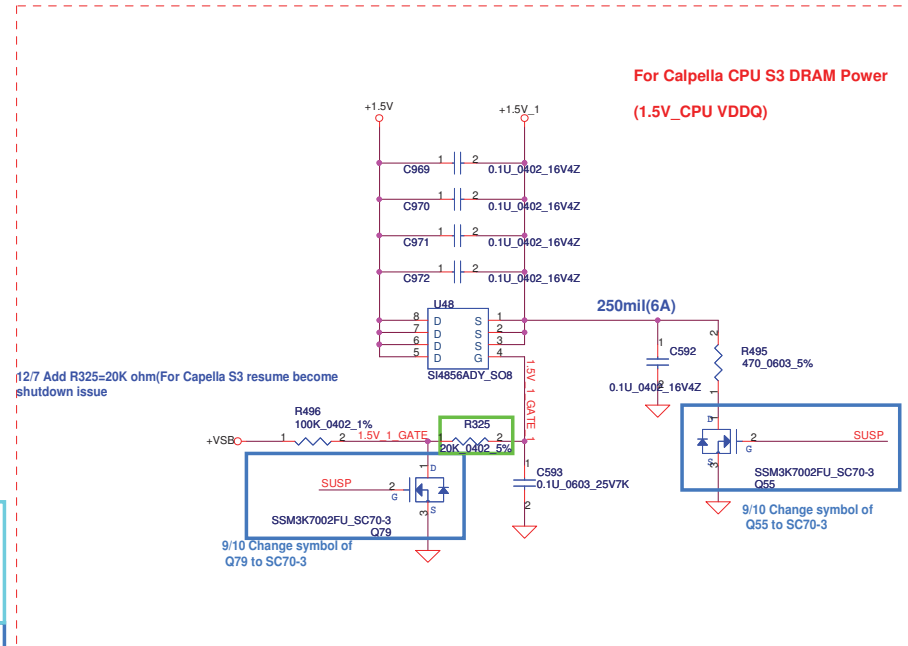
Optional, if +1.5VS can combine with +1.5V_1



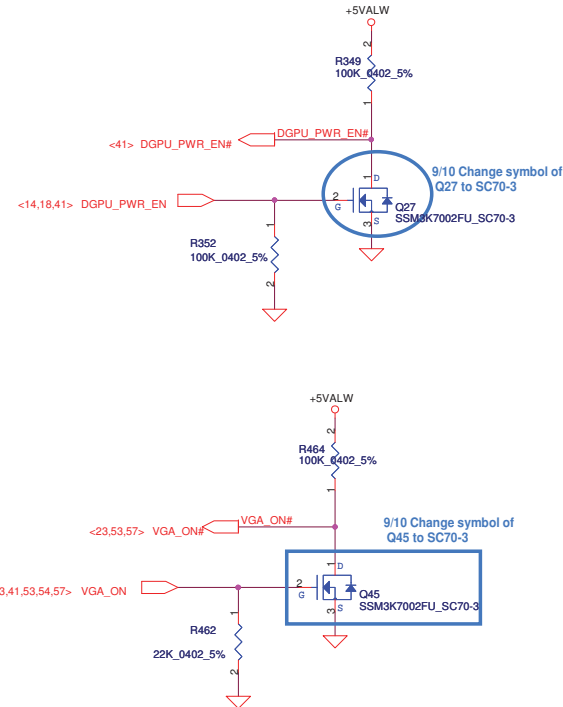
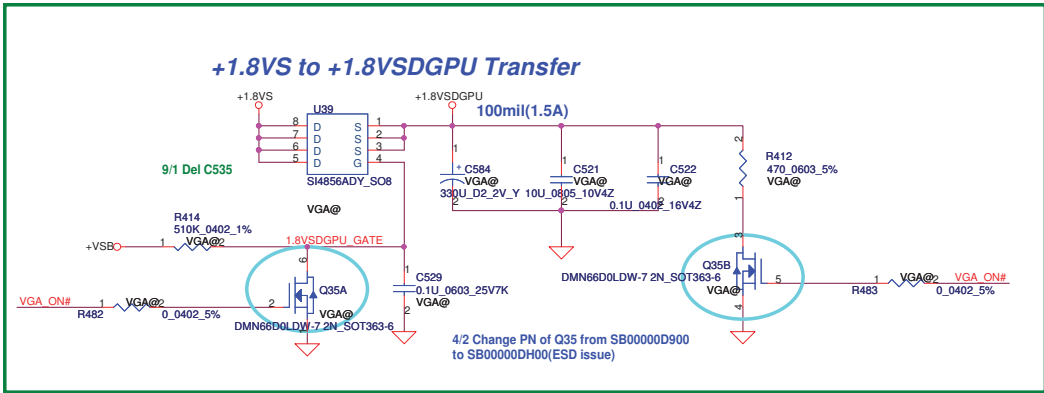
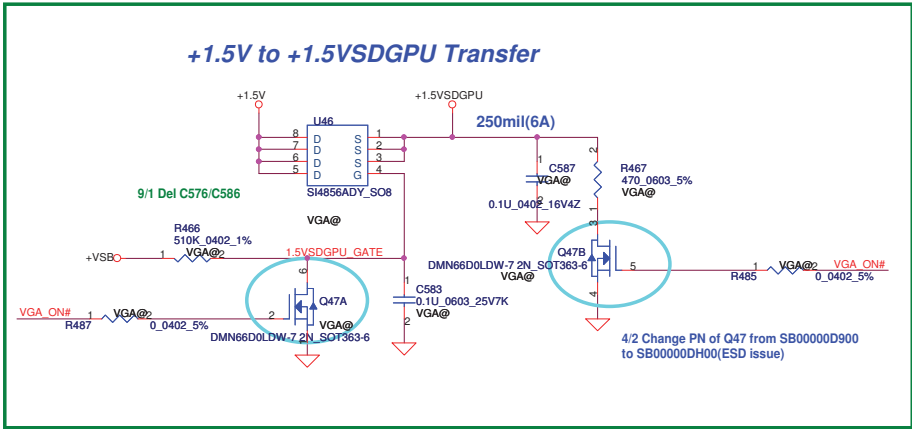
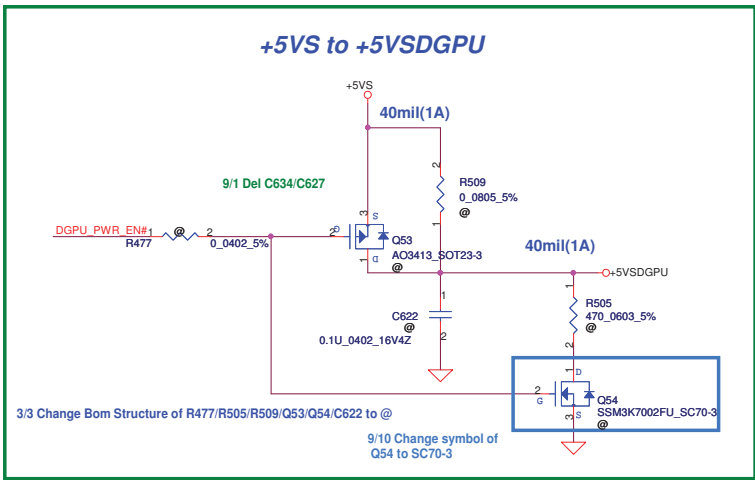
10/9 Delete R428, R431 and Q36
(Remove SBPWR_EN# Function)



For Calpella CPU S3 DRAM Power
(1.5V_CPU VDDQ)

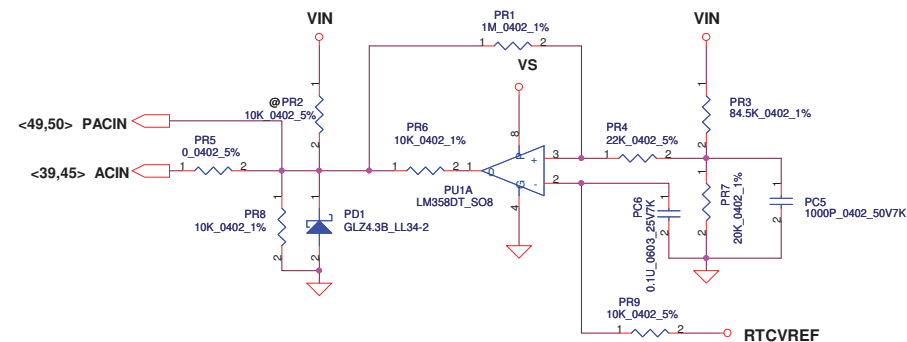
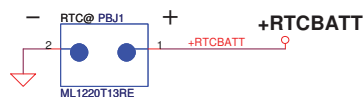
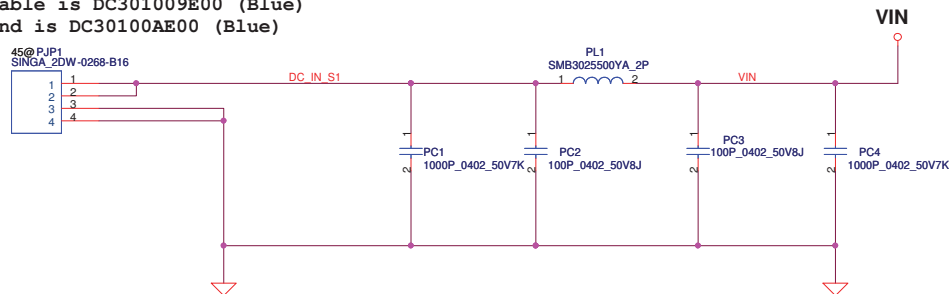


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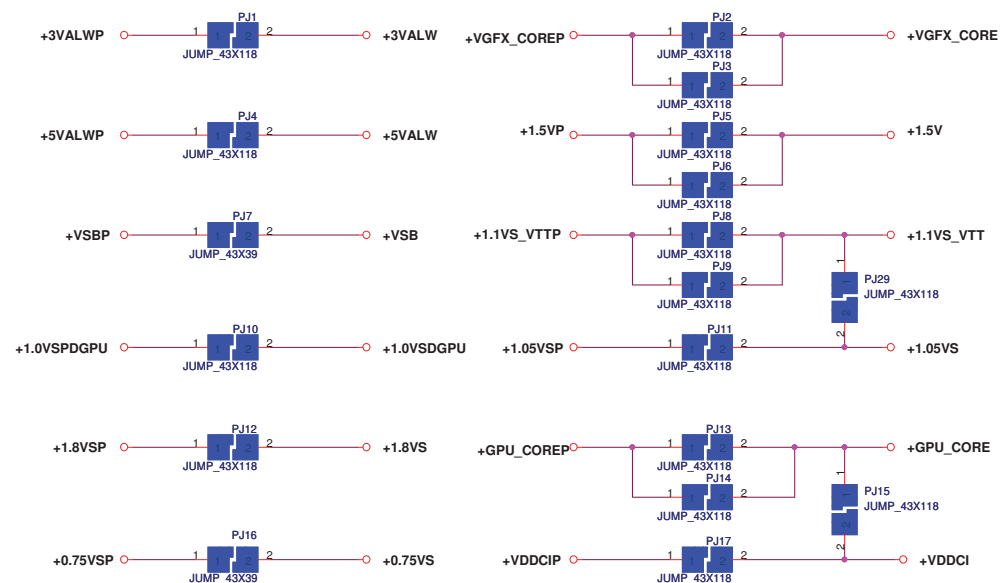
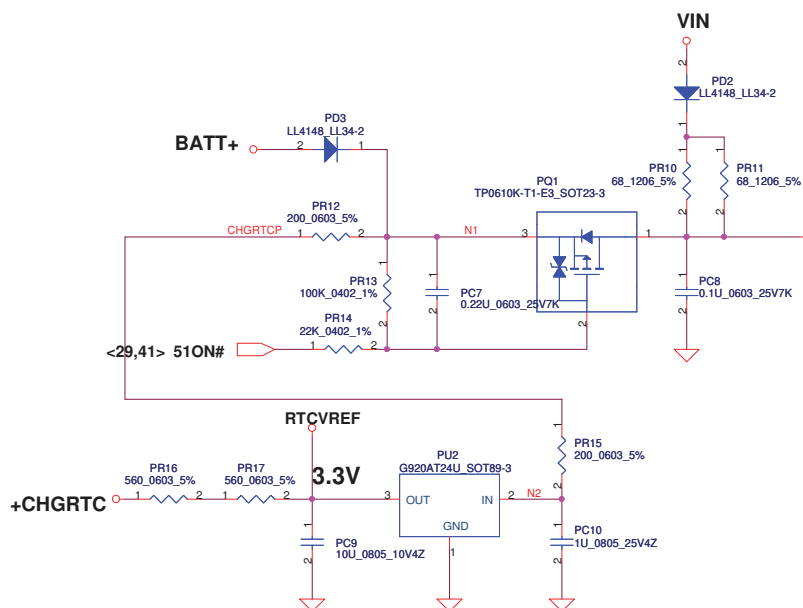
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	
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On board conn is DC301001Y00
Cable is DC301009E00 (Blue)
2nd is DC30100AE00 (Blue)

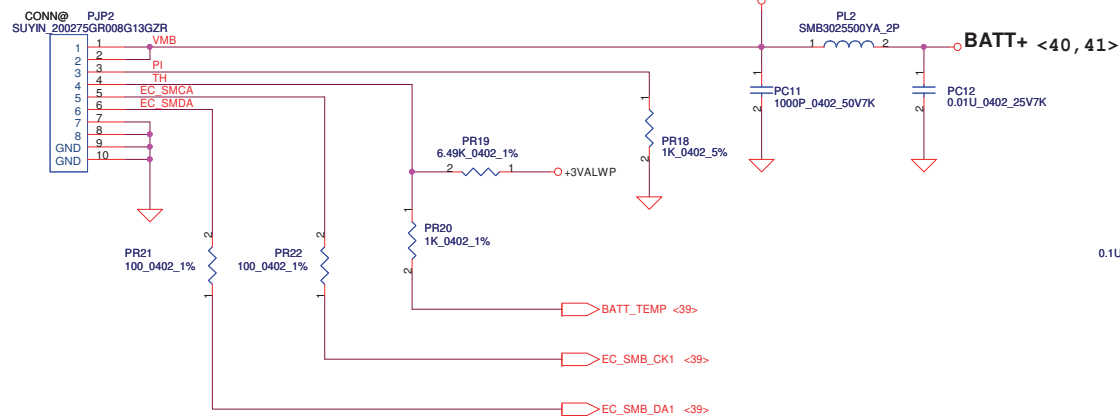


Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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						Size		Document Number		Rev	
						Customer		NCQF0 M/B LA-5981P Schematic		0.1	
						Date:		Sunday, April 18, 2010		Sheet 47 of 62	



Reference only!! Not SPEC

PH1 under CPU botten side :

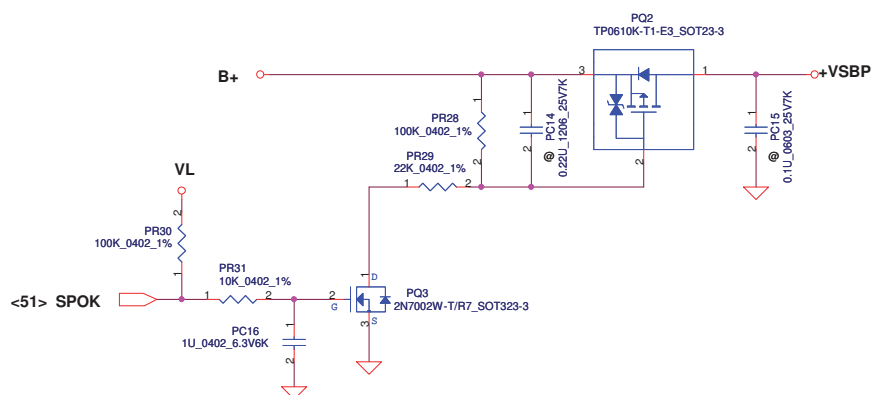
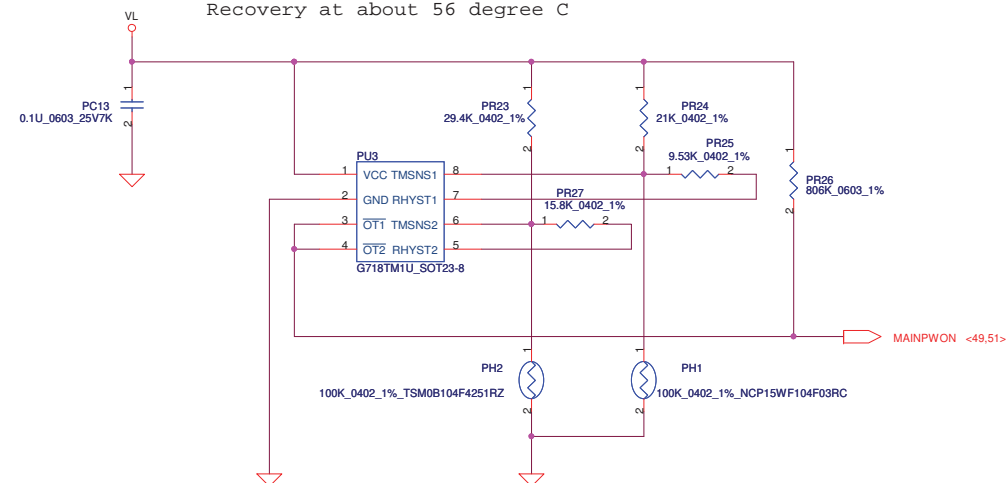
CPU thermal protection at about 92 degree C

Recovery at about 56 degree C

PH2 under FAN down side :

CPU thermal protection at about 82 degree C

Recovery at about 56 degree C



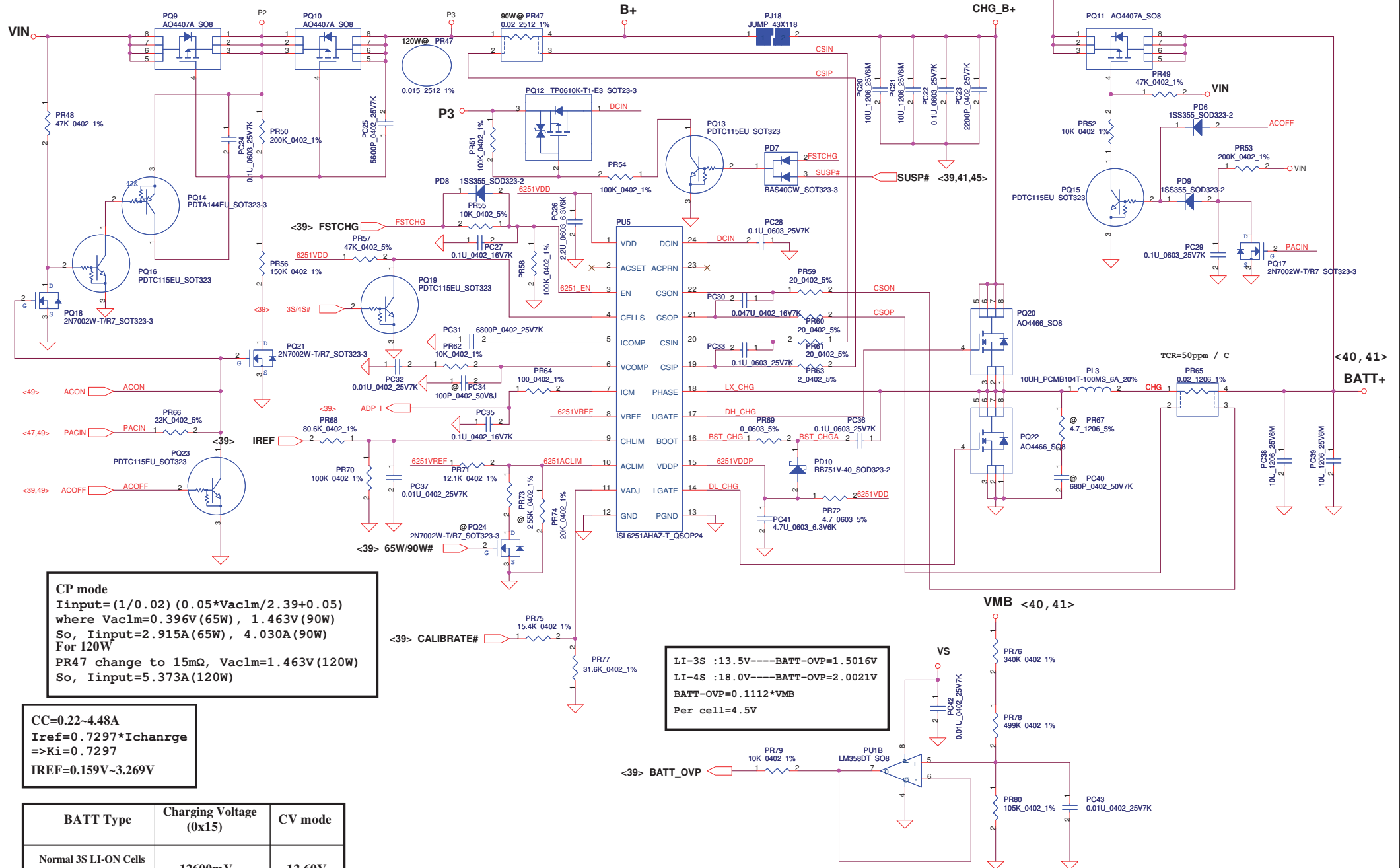
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Issued Date		2009/08/25		Title	
		Deciphered Date		BATTERY CONN / OTP	
				Size	
				Custom	
				NCQF0 M/B LA-5981P Schematic	
				Rev	
				0.1	
				Date:	
				Sunday, April 18, 2010	
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				48 of 62	

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Iada=0~4.74A (90W/19V=4.737A)
Iada=0~3.42A (65W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

90W: CP = 85%*Iada ; CP = 4.026A
65W: CP = 85%*Iada ; CP = 2.908A

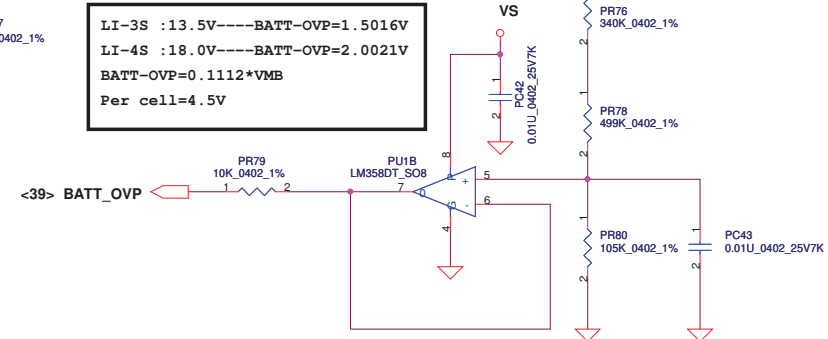


CP mode
Iinput=(1/0.02) (0.05*Vaclm/2.39+0.05)
where Vaclm=0.396V (65W), 1.463V (90W)
So, Iinput=2.915A (65W), 4.030A (90W)
For 120W
PR47 change to 15mΩ, Vaclm=1.463V (120W)
So, Iinput=5.373A (120W)

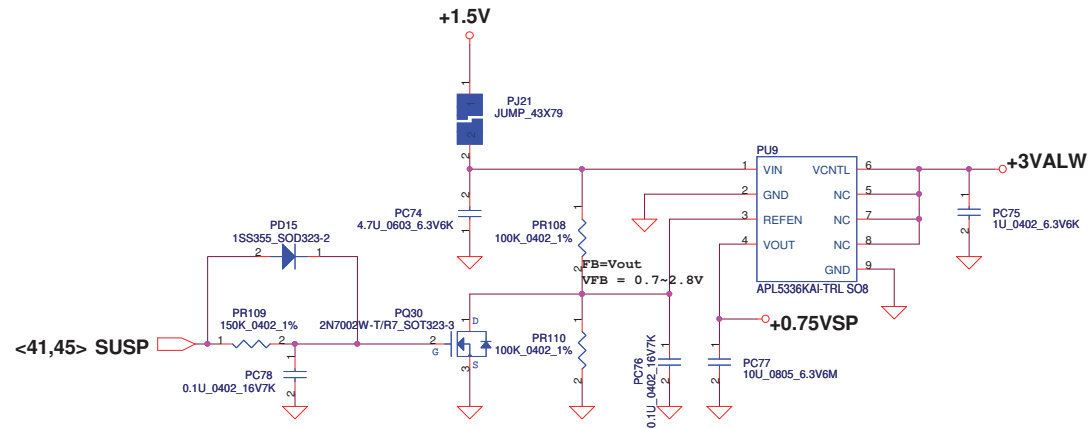
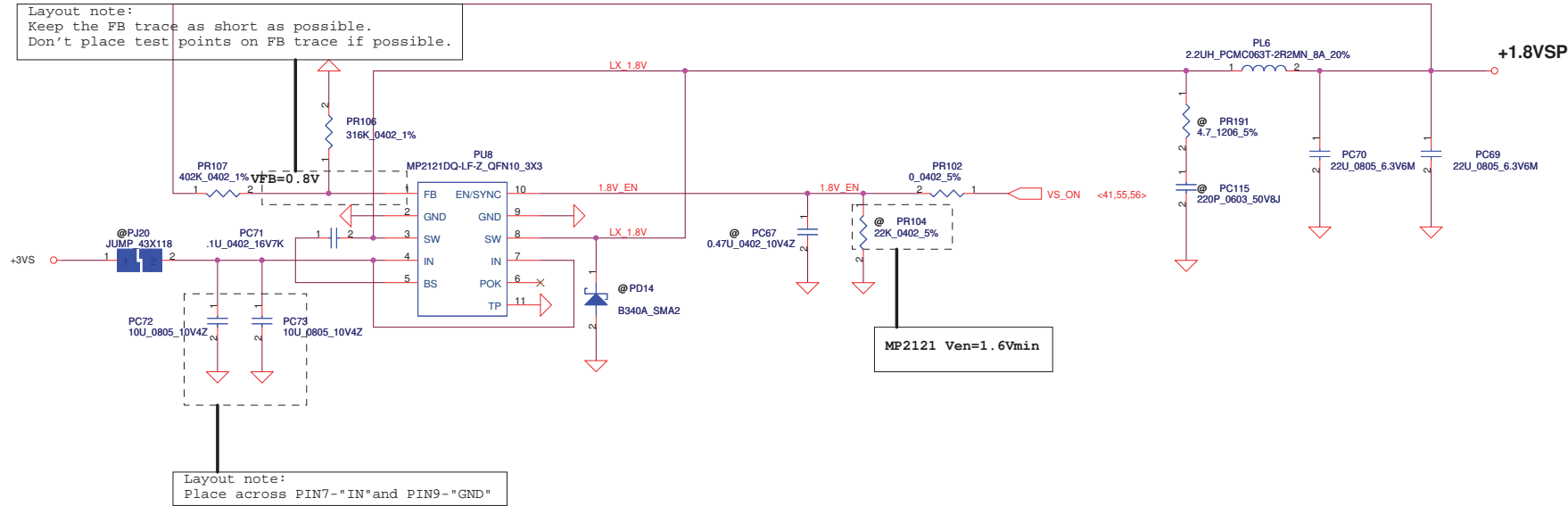
CC=0.22~4.48A
Iref=0.7297*Icharge
=>Ki=0.7297
IREF=0.159V~3.269V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

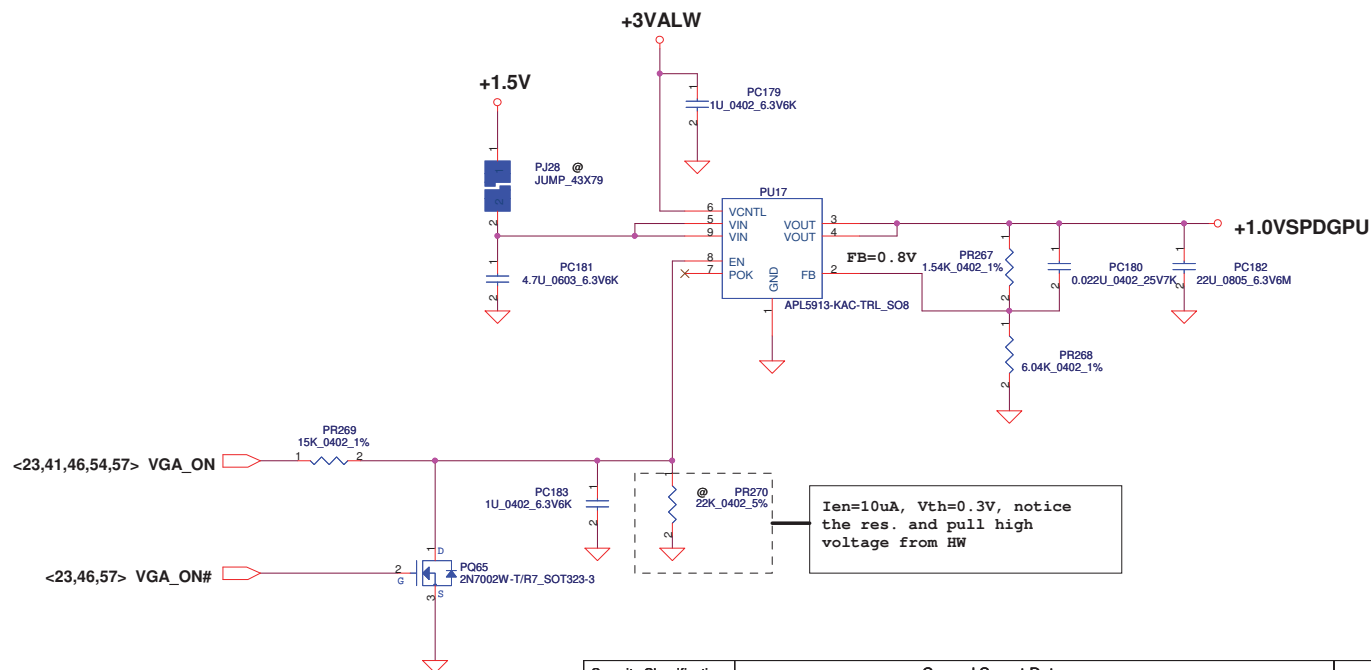
LI-3S : 13.5V----BATT-OVP=1.5016V
LI-4S : 18.0V----BATT-OVP=2.0021V
BATT-OVP=0.1112*VMB
Per cell=4.5V



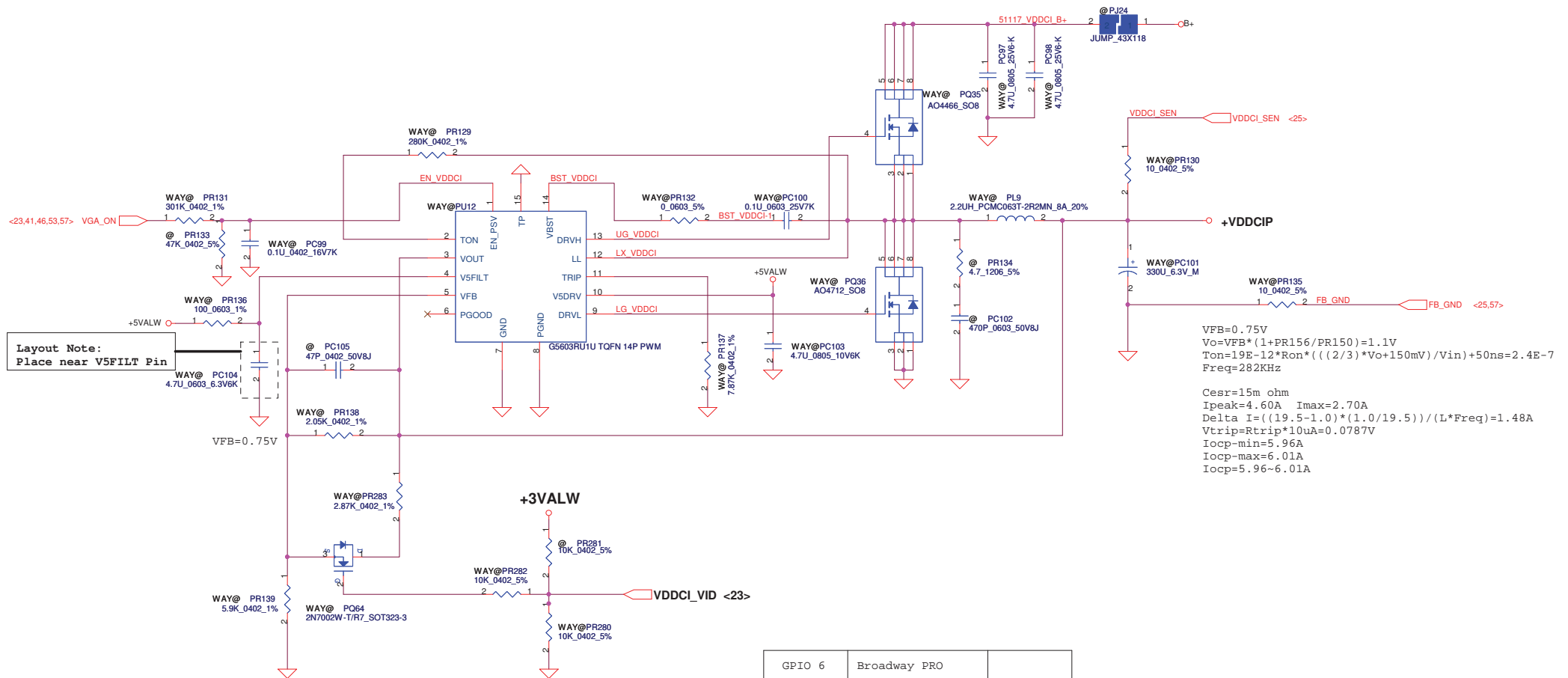
Layout note:
Keep the FB trace as short as possible.
Don't place test points on FB trace if possible.



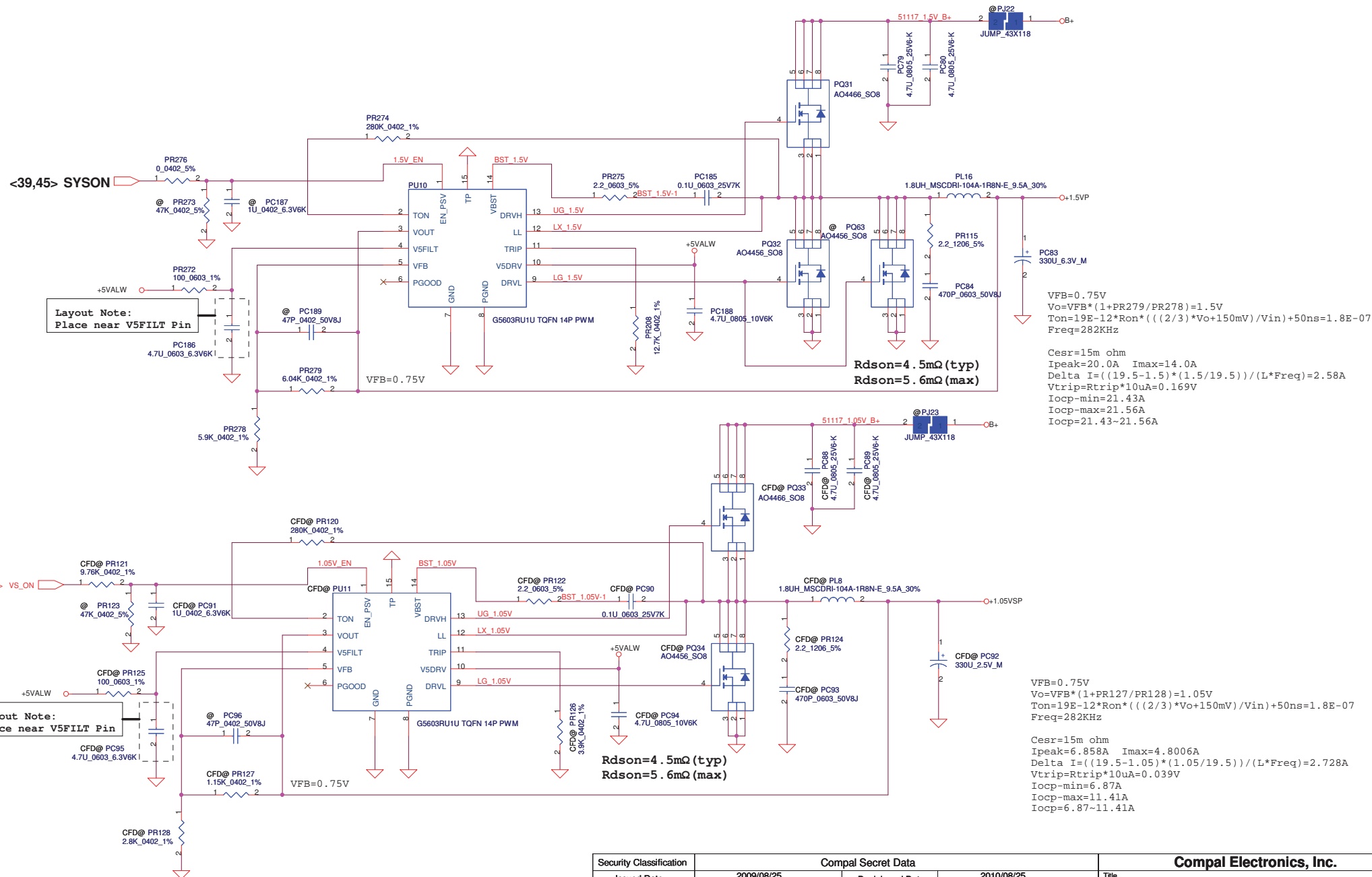
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Size	Custom	Document Number	Rev	Date	
NCQF0		M/B LA-5981P Schematic		Sunday, April 18, 2010	
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62		0.1			



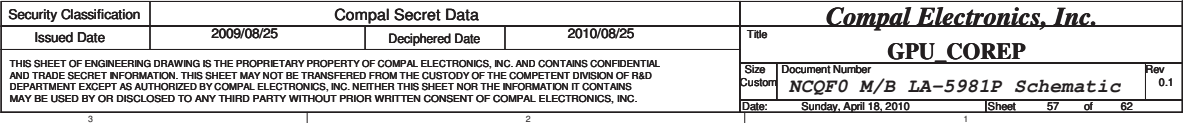
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Size	Document Number	Rev			0.1
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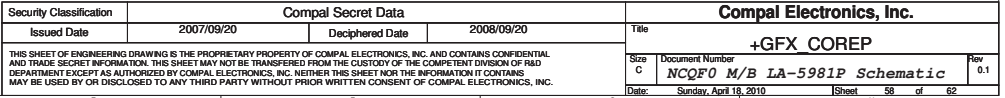


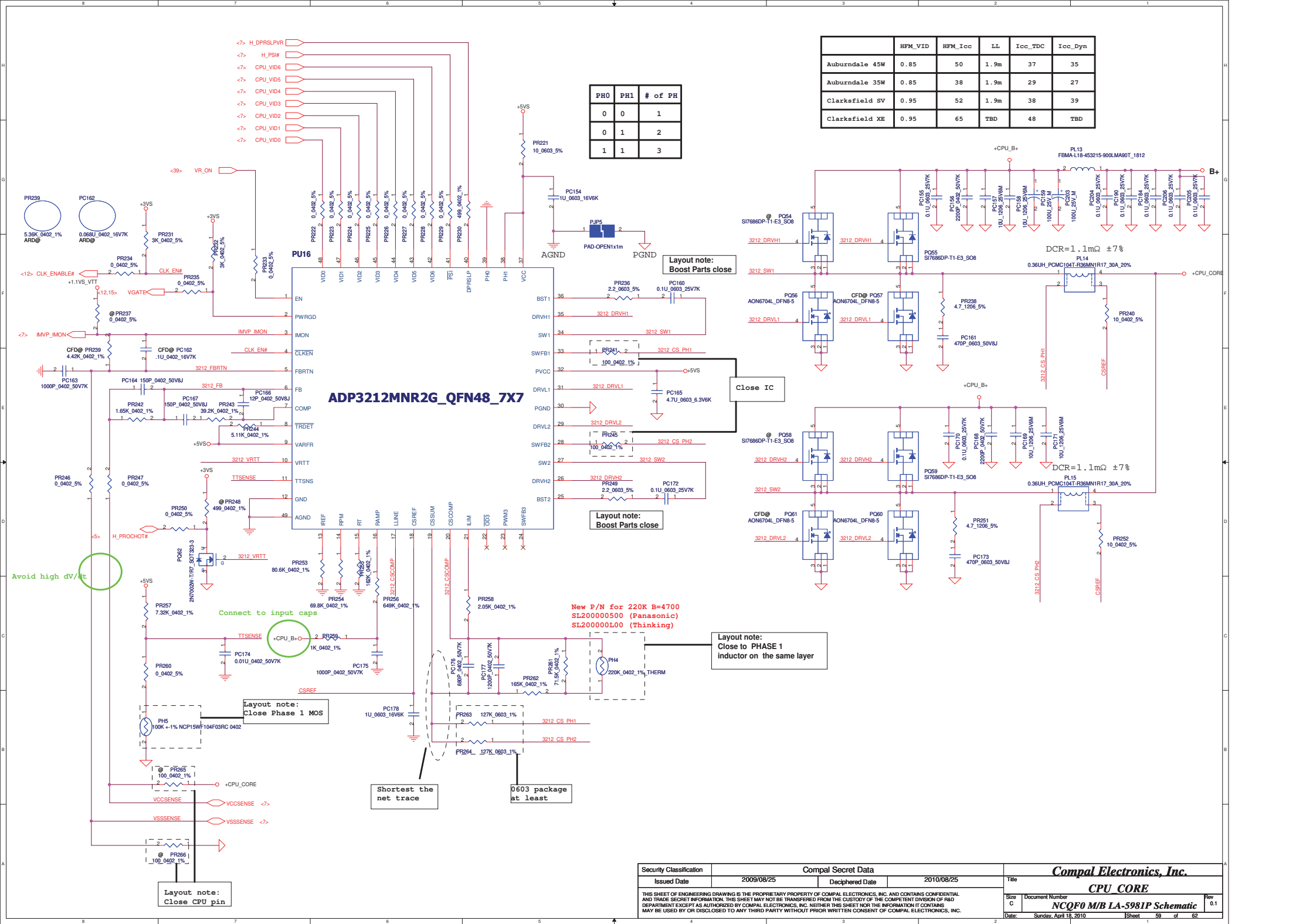
GPIO 6	Broadway PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	



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				Size	Document Number	NCQF0 M/B LA-5981P Schematic		Rev
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	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	0.85	50	1.9m	37	35
Auburndale 35W	0.85	38	1.9m	29	27
Clarksfield SV	0.95	52	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

PH0	PH1	# of PH
0	0	1
0	1	2
1	1	3

Security Classification	Compal Secret Data			<i>Compal Electronics, Inc.</i>		
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				NCQF0 M/B LA-5981P Schematic		
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Version change list (P.I.R. List)

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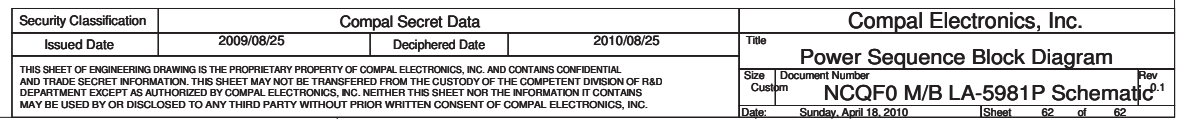
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify chager circuit	Design change	0.1	48	Change BQ24751 to ISL6251	2009 10/07	EVT
2	During shutdown, GFX has a pulse	Make GFX_EN pull down quickly	0.1	58	Add PD15 to connect GFX_EN and VS_ON	2009 11/02	EVT
3	Park XT SPEC change	More display performance	0.1	57	Change PR176 from 31.6KΩ to 43.2KΩ(SD034432280) Change PR179 from 9.53KΩ to 8.87KΩ(SD034887180) Change PR181 from 64.9KΩ to 25.5KΩ(SD034255280)	2009 11/05	EVT
4	ME height not enough	Prevent EL-cap. to knock the door	0.1	51	Change PC56 from 330uF 6L to 220uF 4.5L(SF000002Y00)	2009 11/11	EVT
5	Cost review	Cost down	0.1	57	Change PC124 from 6mΩ to 10mΩ(SF000002O00)	2009 11/11	EVT
6		Tune OCP	0.1	58	Change PR294 from 6.98KΩ to 7.15KΩ(SD034715180) Change PR299 from 10.7KΩ to 11KΩ(SD034110280)	2009 11/11	EVT
7		Tune OCP & Imon	0.1	59	Change PR239 from 499KΩ to 4.53KΩ(SD034453180) Change PC162 from 0.082uF to 0.1uF(SE076104K88) Change PR258 from 1.91KΩ to 2.05KΩ(SD034205180) Change PR261 from 73.2KΩ to 71.5KΩ(SD034715280) Change PR263, PR264 from 120KΩ to 127KΩ(SD014127380) Change PR258 from 1.91KΩ to 2.05KΩ(SD034205180)	2009 11/11	EVT
8							
9	Not enough space	Not enough space	0.1	52	Change PL6 from 10x10 to 7x7(SH000006I80)	2009 11/12	EVT
10	HW Jason request	Add new VGA voltage table	0.1	57	Add PR176,PR179,PR181 virtual parts	2009 11/19	EVT
11	Design review	1.5V change APW7138 to TPS51117	0.1	55		2009 11/19	EVT
12	Design review	Provide GFX output a reference	0.1	58	Add PR310,PR311	2009 12/03	EVT
13	S3 resume shutdown	Make sure 0.75V high later than 1.5V and low earlier than 1.5V	0.1	52	Add PD15	2009 12/08	EVT
14	Design review	1.5V tune output voltage	0.2	55	Change PR278 from 59KΩ to 124KΩ(SD034124380) Change PR279 from 24KΩ to 124KΩ(SD034124380) Change PR208 from 9.09KΩ to 16.9KΩ(SD034169280)	2009 12/15	DVT
15	Power OFF sequence	+1.0vsdgpu need power down within 20ms	0.2	53	Add PQ65	2010 01/05	DVT
16	HW request raise 1% voltage	1.5V tune output voltage	0.2	55	Change PR279 from 124KΩ to 127KΩ(SD034127380)	2010 01/07	DVT
17	OTP activity	Have a pull high	0.2	48	Enable PR23	2010 01/07	DVT
18	EMI solution	Add bypass cap from B+ to Gnd	0.2	59	Add PC184,PC190,PC204,PC205,PC206	2010 01/08	DVT
19	GFX character	Improve Imon, Loadline	0.2	58	Change PR294 from 7.15KΩ to 7.32KΩ(SD034732180) Change PR308 from 43.2KΩ to 53.6KΩ(SD034536380)	2010 01/08	DVT
20	CPU character	Improve Imon, Loadline, Transient	0.2	59	Change PR239 from 4.53KΩ to 4.42KΩ(SD000004J80) Change PC176 from 390pF to 680pF(SE074681K80)	2010 01/08	DVT
21	Costdown	Change pack from 1206 to 0805	0.2		Change PC79,PC80,PC88,PC89,PC97,PC98 from 1206 to 0805(SE000006R80)	2010 01/08	DVT
22	Tune sequence	GPU_core need ramp up before VDDCIP	0.2	54	Change PR131 from 10KΩ to 57.6KΩ(SD034576280)	2010 01/08	DVT
23	Run 3D Mark hang	Improve GPU character	0.2	57	Change PLL1 from 0.56uH to 0.36uH(SH000005680) Change PR169 from 2.43KΩ to 3.92KΩ(SD034392180) Change PR176 from 31.6KΩ to 25.5KΩ(SD034255280) Change PR181 from 64.9KΩ to 64.9KΩ(SD034649280) Change PR137 from 6.65KΩ to 7.87KΩ(SD034787180)	2010 01/13	DVT

Delete
2009
11/05

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5		4		3		2		1	
NO DATE		PAGE		MODIFICATION LIST		PURPOSE			
01/05		P.40		PWR_LED# connect from +3VALW to +3VS; PWR_SUSP_LED# conector from +3VS to +3VALW					
01/05		P.10		JDIMM1 and JDIMM2 location swap					
01/05		P.47~60		upgrade PWR schematic					
01/06		P.31		Change net name of Q85.pin2/5 from +3VS to +3VS_DELAY					
01/06		P.35		Add one Lid Switch schematic for reserve					
01/08		P.47~60		upgrade PWR schematic					
01/08		P.42		Add two of 300 ohm bead for DMIC_CLK and SPDIF signal(L6/L8)					
01/11		P.47~60		upgrade PWR schematic					
01/11		P.40		Reserve R120=300 ohm pull-high to +3VALW					
01/11		P.18		Change net name of Q23.pin2 from VGA_HDMI_DET to HDMI_HPD					
01/12		P.25		Add C602=330uF to decrease ripple of +GPU_CORE					
02/25		P.23		Change net connection(from R45.2 to Q7.1)					
02/25		P.29		Add R37=SG@ 0 ohm connect between DPST_PWM_1 and INVTPWM					
02/25		P.34		Add C936~C938=mount 0.1uF for slove EMI issue					
02/25		P.39		Add R430/R442/R446=mount 10k ohm pull-high to +3VALW					
02/25		P.39		Change Bom structure of R421/R422/R431 from mount to reserve					
02/25		P.47~63		upgrade PWR schematic					
03/01		P.5		Del XDP schematic(JP5/R89/R92/R93/R96/C168/R86/R657/R663)					
03/01		P.14		Add R326/R345/R782/R796(for use JMB380 Ver.C)					
03/01		P.14		Add Q49/Q50(for use JMB380 Ver.C)					
03/01		P.47~63		upgrade PWR schematic					
03/02		P.37		Add R718/C168 (for reset)					
03/31		P.23		Add Update VRAM Table					
03/31		P.43		Change value of R4 from 4.7K ohm to 5.62K ohm					
03/31		P.43		Change value of C3 from 0.1uF to 0.033uF					
03/31		P.36		Change Bom structure of R654/R658/R280/R281/R324/R331 from mount to @					
03/31		P.36		Change Bom structure of L32/L33/L69 from @ to mount					
03/31		P.36		Change symbol and PN of L32/L33/L39 from SM070001310 to SM070000K00					
03/31		P.24		Change Bom structure of R83 from SG@ to MAD@					
04/01		P.39		Change footprint of SW2/SW3 from SW_SKRELGE010_2P to SW_NTC317-AB1G-C220C_2P					
04/02		P.23		Change PN of Q9 from SB00000D900 to SB00000DH00					
04/02		P.29		Change PN of Q6/Q80/Q81 from SB00000D900 to SB00000DH00					
04/02		P.30		Change PN of Q84 from SB00000D900 to SB00000DH00					
04/02		P.31		Change PN of Q85 from SB00000D900 to SB00000DH00					
04/02		P.31		Change PN of Q61 from SB570020110 to SB000008J10					
04/02		P.43		Change PN of Q69 from SB00000D900 to SB00000DH00					
04/02		P.45		Change PN of Q40/Q41/Q42/Q43 from SB00000D900 to SB00000DH00					
04/02		P.46		Change PN of Q35/Q47 from SB00000D900 to SB00000DH00					
04/15		P.39		Change PN of SW2/SW3 from SN100001C00 to SN100003R00					
04/15		P.41		Change Bom structure of SW1 from mount to @					
04/18		P.29		Add LVDS schematic(U13/U31/C204/C187=@)					
04/18		P.40		Add R51=@ 0 ohm					
04/18		P.47~63		upgrade PWR schematic					
5		4		3		2		1	

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	EMI request	Cut-in snubber and couple cap on B+	0.2		Enable 3V/5V/1.5V/1.05V/VTT/GPU snubber	2010 01/13	DVT
25	Buyer request	Costdown	0.2		Change PU10,PU11,PU12 from TPS51117 to G5603(SA00003HM00)	2010 01/14	DVT
26	HW/Ivan request	Raise voltage 2%(Arrendale only)	0.3	56	Change PR153 from 4.99K Ω to 5.36K Ω (SD034536180)	2010 02/11	PVT
27	The same setting for 2nd source	Fix 5V for all IC	0.3	51	Disable PR87	2010 02/23	PVT
28	GPU output cap add 330uF for hang issue	Tune VDDCIP sequence and Power common design	0.3	54	Change PR131 from 57.6K Ω to 301K Ω (SD034301380) Net +5VALW instead of +5VSDGPU	2010 02/23	PVT
29	EMI request	Cut-in snubber and boost res.	0.3		Change PR122,PR142,PR236,PR249,PR275 from 0 Ω to 2.2 Ω (SD013220B80) Add PR238,PR251 to 4.7 Ω Add PC161,PC173 to 470pF	2010 02/25	PVT
30	65/90# only low signal	Fix adapter mode	0.4	50	Disable PR73, PQ24	2010 03/23	Pre-MP
8	Protect logic deformation	Add PH2 function	0.4	48	Change PR23 from 0 Ω to 29.4 Ω (SD034294280) Add PR27, PH2	2010 03/23	Pre-MP
9	Improve anti-noise	Reduce voltage divider	0.4	54	Change PR138 from 43K to 2.05K(SD034205180) Change PR139 from 124K to 5.9K(SD034590180) Change PR283 from 60.4K to 2.87K(SD034287180)	2010 03/26	Pre-MP
10	Improve anti-noise	Reduce voltage divider	0.4	55	Change PR278 from 124K to 5.9K(SD034590180) Change PR279 from 127K to 6.04K(SD034604180) Change PR127 from 24K to 1.15K(SD034115180) Change PR128 from 59K to 2.8K(SD034280180)	2010 03/26	Pre-MP
11							
12	Cut-in 120W adapter	Tune a CP setting for 120W adapter	0.4	50	Change PR47 from 0.02 to 0.015(SD000001E00)	2010 03/26	Pre-MP
13	Modify VGA voltage table	Rise Broadway voltage to the same to Park	0.4	57	Change PR179 from 9.53 to 8.87 Change PR181 from 64.9 to 43.2	2010 04/16	Pre-MP
14							
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